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FINAL REPORT

DEVELOPMENT OF A HIGH SPEED POWER THYRISTOR -
THE GATE ASSISTED TURN-OFF THYRISTOR

by

D. R. Hamilton, J. Brewster, D. Frobenius and T. Desmond

WESTINGHOUSE ELECTRIC CORPORATION
Semiconductor Division
Youngwood, Pennsylvania 15697

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Project Managers Dr. Francis C. Schwarz and Julian F. Been,
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16. Abstract

A high speed power switch with unique turn-off capability was developed. This gate assisted turn-off thyristor was rated at 600V and 50A with turn-off times of 2μs. Twenty-two units were delivered for evaluation in a series inverter circuit. In addition, test circuits designed to relate to the series inverter application were built and demonstrated. In the course of this work it was determined that the basic device design is more than adequate to meet the specifications. However, improvements and/or changes in fabrication technology, which may impact device design, must be made in order to effect a manufacturable device as well.

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FOREWORD

The research described herein was done by the Westinghouse Electric Corporation, Semiconductor Division, Youngwood, Pa., on Contract NAS 12-2198. The work was started under Drs. F. C. Schwarz and C. A. Renton, formerly of the NASA Electronics Research Center, 575 Technology Square, Cambridge, Massachusetts, and completed under Dr. F. C. Schwarz and Mr. J. F. Been, NASA Lewis Research Center, Cleveland, Ohio.

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A. CONTRACT OBJECTIVE

The objective of this contract was to develop a thyristor type of switch that will recover its forward current blocking capability within 2 microseconds when used in a series inverter.

B. SUMMARY OF PERFORMANCE TOWARD THE CONTRACT REQUIREMENTS

Westinghouse has successfully accomplished the objective of the contract and completed the work requirements stated in Section C of the contract. The work statement includes four items, which are discussed below in sequence:

Item 1 -- To formulate a philosophy of thyristor design consistent with the objective of meeting the following specifications:

Max. Forward and Reverse Blocking Voltage	V_{max}	600V
Max. Anode Current	I_{av}	50A
Recovery Time		2 μs
dv/dt		400V/μs
V_f		2V @ 50A

Such a design was formulated and devices were made and delivered in accordance with Item 2 below.

Item 2 -- Device fabrication. The original contract calling for ten (10) devices was extended and the required number was increased by twelve (12), making a total of twenty-two (22) units in all. These twenty-two (22) units were delivered along with an additional two (2) units to be used for display purposes. Of the twenty-two (22) good units, nineteen (19) met all of the

specifications stated in Item 1 above, one (1) unit met the requirements except for V_F, which was 2.3 volts at 50 amps rather than the desired value of 2.0 volts at 50 amps, and two (2) had low reverse blocking voltage at 100°C. In view of the difficulty experienced in making thyristor type switches that will recover their forward current blocking capability within two microseconds, Westinghouse feels that such minor deviations from the V_F and voltage specifications are acceptable within the limits expected for a development contract of this type and that the contract requirements have been met.

Item 3 -- Test circuits. The required testing circuits were built and performed in an entirely acceptable manner. The circuits were specifically designed to relate to the series inverter of Schwarz, discussed in Section 1.2 of this report, and units so tested are expected to perform adequately in that circuit when it is built.

Item 4 -- Identification of areas for future investigation. This item is discussed more completely in a later section. In summary, the problem areas relate particularly to the manufacturability and encapsulation of the device. The basic design of the npnp silicon sandwich from which the device is fabricated has proved to be more than adequate. The problems encountered in the fabrication, however, dictate a minor but -- in terms of manufacturability -- significant departure from the mesa structure now employed. These problem areas are well defined because of the present contract and future work should result in a completely manufacturable device.

Westinghouse has also met the terms of the contract in the delivery of reports and in Inspection and Acceptance criteria.

C. RECOMMENDATIONS FOR FUTURE WORK

A natural recommendation for future effort on the gate assisted turn-off thyristor (GATT) device is the extension of the device capability to higher levels in terms of blocking voltage, current handling capability, and switching speed. The results of the present effort, however, show that a careful re-examination of the process techniques should accompany any further development efforts.

Four types of process problems were encountered during the contract work.

1) Cathode Mesas
   a) the mesa formation itself,
   b) cathode mesa leakage currents, and
   c) contacting of the mesas.

2) Diffusion
   a) control of bulk lifetime, and
   b) reproducibility of the p-diffusion

3) Blocking Voltage
   Degradation induced by non-optimum processing
   and encapsulation.

4) Device Encapsulation
   In its detailed interaction with the selected mesas.

All of these problem areas are fabrication/processing problems. Although they do indeed impact the device design, the net effect must be considered as a yield problem since the devices that were successfully completed did, in fact, meet specification, and improvements in parameter performance can be projected based on well known principles of PNPN device design.

To approach the fabrication problems, we recommend that:

1) The cathode-gate junctions be prepared by a planar technique, obviating present problems in control of the mesa etch, the cathode-gate geometry, and various mesa etch mask defects.

2) All of the junctions be provided with an inorganic passivation.

3) Thick cathode and gate metallization techniques be developed to relieve packaging stress problems.

4) Devise more reproducible p-diffusion and lifetime control processes.

5) Improve package design to relieve local stress problems.

1. INTRODUCTION

1.1 Power Processing

A broad area of the field of power processing deals with the conversion of dc power from one level of voltage to another. In some systems, the prime power is supplied by relatively low voltage exotic sources producing dc output voltages too low and too variable to be used directly. In others, the dc source is the rectified output of an ac line which must be adjusted to the desired voltage level and then regulated at that point.

Much technology has been generated in this field, making possible a solution to almost any system problem presented. However, when examined critically from the standpoints of equipment size, weight, reliability, and efficiency, each circuit solution represents a certain compromise of desired properties. It is always desirable, therefore, to advance the art with new technology which offers an improved compromise of the system evaluation criteria described.

Circuits for the conversion of dc power from one level to another must of necessity interrupt dc currents. This can be done by inserting an active switching device in the dc line, or alternatively by utilizing an energy storage device. At present, no solid-state dc switch is available for use at high power levels, so the technique normally used for the former is to force commutate a thyristor. This technique, although feasible, results in high energy transients which are detrimental to efficiency and reliability, and contribute heavily to undesirable electromagnetic interference. Circuits of this type also suffer disadvantages in size and weight and are limited in internal operating frequency by the recovery times of the thyristors, which are rather long.

A more desirable circuit configuration employs lossless energy storage devices, such a inductors and capacitors, to effectively interrupt dc currents by natural commutation. In such circuits, solid-state devices without turn-off properties, such as thyristors, may be employed without the need for commutating circuitry. Because commutation takes place naturally, no large voltage or current transients need occur, increasing reliability and efficiency.

Circuits of this type do work well and exhibit all of the previously discussed advantages. They are, however, limited in size and weight by the maximum internal carrier frequency, which is in turn limited by the relatively long recovery times of the thyristors used. A considerable improvement in circuit performance would result from the use of a solid-state switching device which, upon current interruption by external means, would require only a short interval before forward voltage may be reapplied. It need not include the ability to interrupt current by application of a gate signal.

The gate assisted turn-off thyristor (GATT) is such a device. It was developed on this contract.

1.2 The Series Inverter

The intended use for the GATT device of this contract is a series inverter circuit. Although the device proposed will be useful in any series inverter configuration, it will be assumed for the purposes of this program that the specific circuit under consideration is that described by Schwarz [1,2]. The basic motivation for the system described by Schwarz was the need to develop a power conversion system useful for space application. Of foremost interest in such designs are the considerations of efficiency, power density, and reliability.

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After first studying various solid state switches, it was concluded by Schwarz that resonant circuits are best suited for the utilization of thyristors in power conditioning systems. Of foremost consideration in this selection were the surge capacity of thyristors and the ability to be turned 'on' and 'off' at pulse repetition rates in excess of ten kilohertz, yet with smaller power dissipation than transistors in parallel inverters. Recent advances with thyristors have enabled turn-on at high repetition rates and high rates of rise of current; and, thyristors may be turned off by natural commutation, with low losses in the process.

The dissipation features of thyristors versus transistors were aptly demonstrated by the use of a ten megahertz bandwidth wattmeter.[3] The turn-off dissipation properties of the naturally commutated thyristor thus obtained were instrumental in selection of the series inverter as the power conditioner with which to transform dc power to ac power. The inherent property of the series inverter to provide natural commutation of the thyristor currents results in relatively low thyristor dissipation which is almost independent of the pulse repetition rate at constant duty cycle. The ensuing power dissipation in the thyristor is substantially lower than that normally experienced with transistors or force commutated thyristors. The framework of the inverter efficiency design is then based upon this independence of power dissipation from frequency due to the low dissipation experienced during turn-on and turn-off phases of the switching processes. The selection of the switch then leads to the selection of the circuit which works best with the useful properties of the switch: the thyristor-series inverter combination.

The operating point of the series inverter is next considered from the standpoint of efficiency. Figure 1 shows the series inverter current waveform (i_1). The form factor of the current waveform may be expressed as

1) $\text{Form Factor} = \rho_i = \dfrac{i_{rms}}{i_{av}} = \dfrac{\pi}{2\sqrt{2}}\sqrt{1 + T_d/T_k} = \dfrac{\pi}{2\sqrt{2}}\sqrt{1 + \dfrac{T_d}{\pi}\dfrac{1}{LC}}$
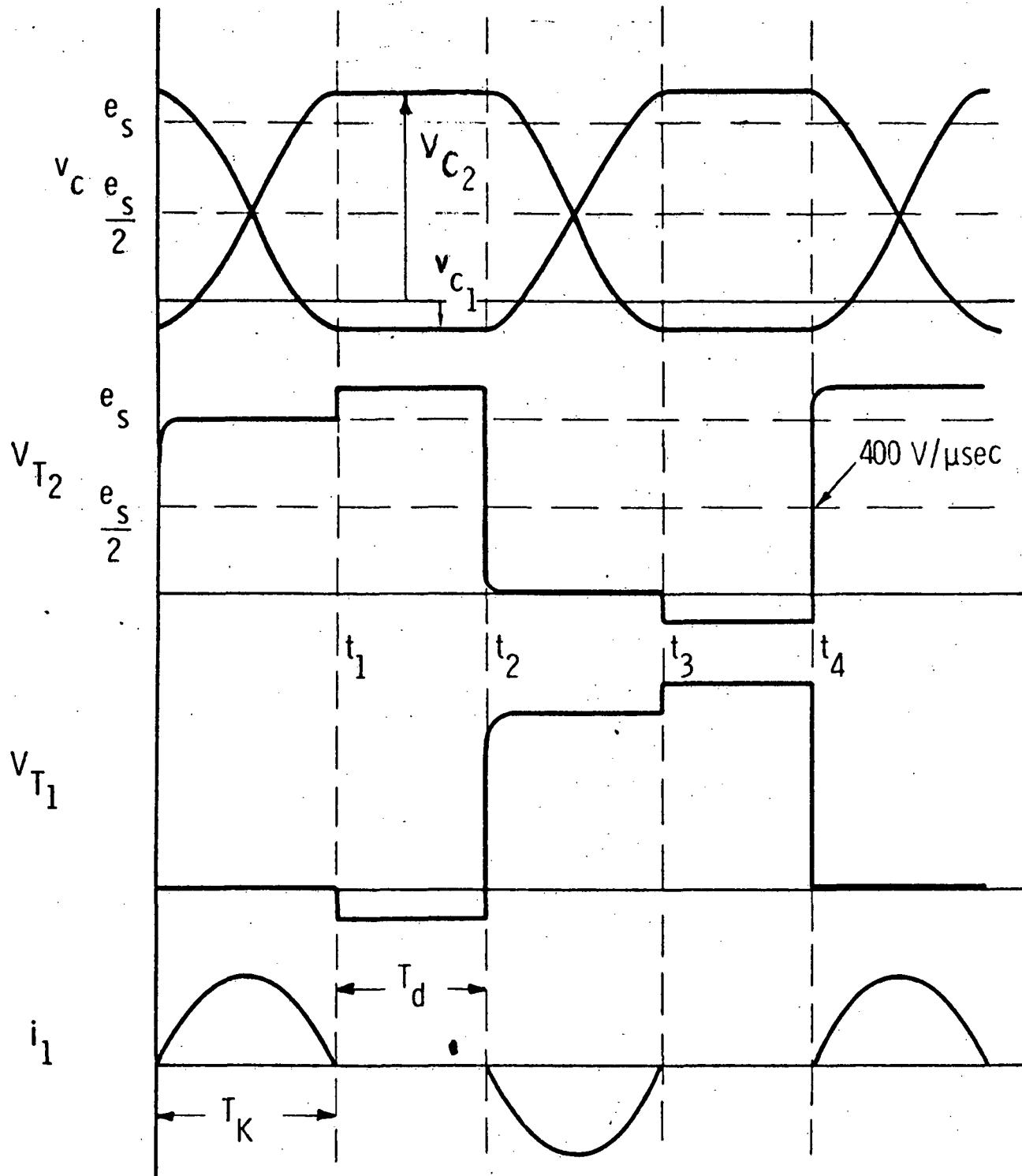
Fig. 1 —Load insensitive series inverter waveforms

J. W. Brewster
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where T_d = delay time between end of conduction of thyristor 1 and start of conduction of thyristor 2.

T_k = half period of the natural resonant frequency of the system = $\sqrt{LC}$ where L and C are equivalent series inductance and capacitance of the series inverter.

From Schwarz, the relative power loss in the system can be approximated by

$$2) \quad 1 - \eta = \rho_i^2 \frac{R_S}{R_L^1 + R_S}$$

where η = the efficiency of the system

R_S = equivalent inverter series resistance

R_L^1 = equivalent inverter load resistance

Once the series inverter design is fixed, losses can be minimized by reducing the current form factor ρ_i. From (1), the form factor is minimized by reduction of T_d which, as already defined, is limited to a greater value than t_{off}, the standard turn-off time of a thyristor under self-commutating performance. Before development of the gate-assisted thyristor, recovery times of conventional thyristors were limited to 10 μs.

Such devices, with 10 μsec turn off time, however, allowed Schwarz to construct a series inverter with efficiency in excess of 95%, power output of 2kW, and power density of 0.4 kW/kg. The purpose of this contract was to develop a thyristor which would recover its forward blocking properties after normal self commutation within 2 μs. With this device, Schwarz contemplates an improved inverter with efficiencies of the order of 95%, similar power output, and power densities of 1 kW/kg. He assumes the series inverter natural frequency could be increased to 50 kHz, and that economies of size will result from the 50 kHz frequency due to reduction of physical size and weight of transformers and of the associated energy storage elements. It is also expected that efficiencies will not deteriorate.

As a concluding point, the availability of high current thyristor switches reduces the need for unreliable paralleling. Thus, the reliability of the Schwarz inverter design has additional merit because the paralleling of groups of solid state switches, with their attendant increase in number, reduces the probability of failures.

A symbolic schematic of the series inverter is shown in Figure 2. Waveforms derived from Figure 2 are shown in Figures 1 & 3. The arrangement is conventional and consists of two series inverter circuits for which components L_1 and load transformer T_1 are shared by both circuits. Operation consists of the alternate sharing of current by switch Th_1 and Th_2. As an example, when Th_1 conducts, C_1 provides half of the load current pulse by discharging from some value greater than e_s to a negative voltage which is some fraction of e_s. At the same time, capacitor C_2 resonantly charges from some negative potential which is some fraction of e_s to a positive value greater than e_s. Capacitors C_1 and C_2 resonate with inductor L_1, and the sum of potentials across C_1 plus C_2 is always e_s. The waveforms in Figure 1 illustrate the sequence of events of the inverter operation. Assuming operation starts at time t_1, then C_2 is charged to $e_s + \Delta v$ and C_1 is charged to $-\Delta v$. At time t_1 thyristor Th_1 is naturally commutated and a delay time $T_d \geq t_{off}$ must exist before Th_2 can be triggered. The delay time of T_d is shown in Figure 1. After the delay time, Th_2 is triggered and at the instant that Th_2 is triggered, Th_1 experiences a rise in anode voltage at a rate which is less than or equal to 400V per microsecond. Capacitor C_2 discharges producing a negative going current pulse through transformer T_1. During the conduction of Th_2, the voltage across C_2 falls resonantly from $e_s + \Delta v$ to $- \Delta v_1$ and the voltage across C_1 rises from $-\Delta v$ to $e_s + \Delta v$. Hence at time t_3 the potentials of C_1 and C_2 have reversed from their position at time t_1. After a delay T_d, thyristor Th_1 conducts, provides a positive current pulse through transformer T_1 and the potentials of C_1 and C_2 return to their values they assumed at time t_1. In this cycle, an ac current pulse was developed through L_1 and transformer T_1. Rectifier RR-1 in the secondary of T_1 reconverts the pulsating current to unipolar pulses which charge C_3 to a level of e_o.
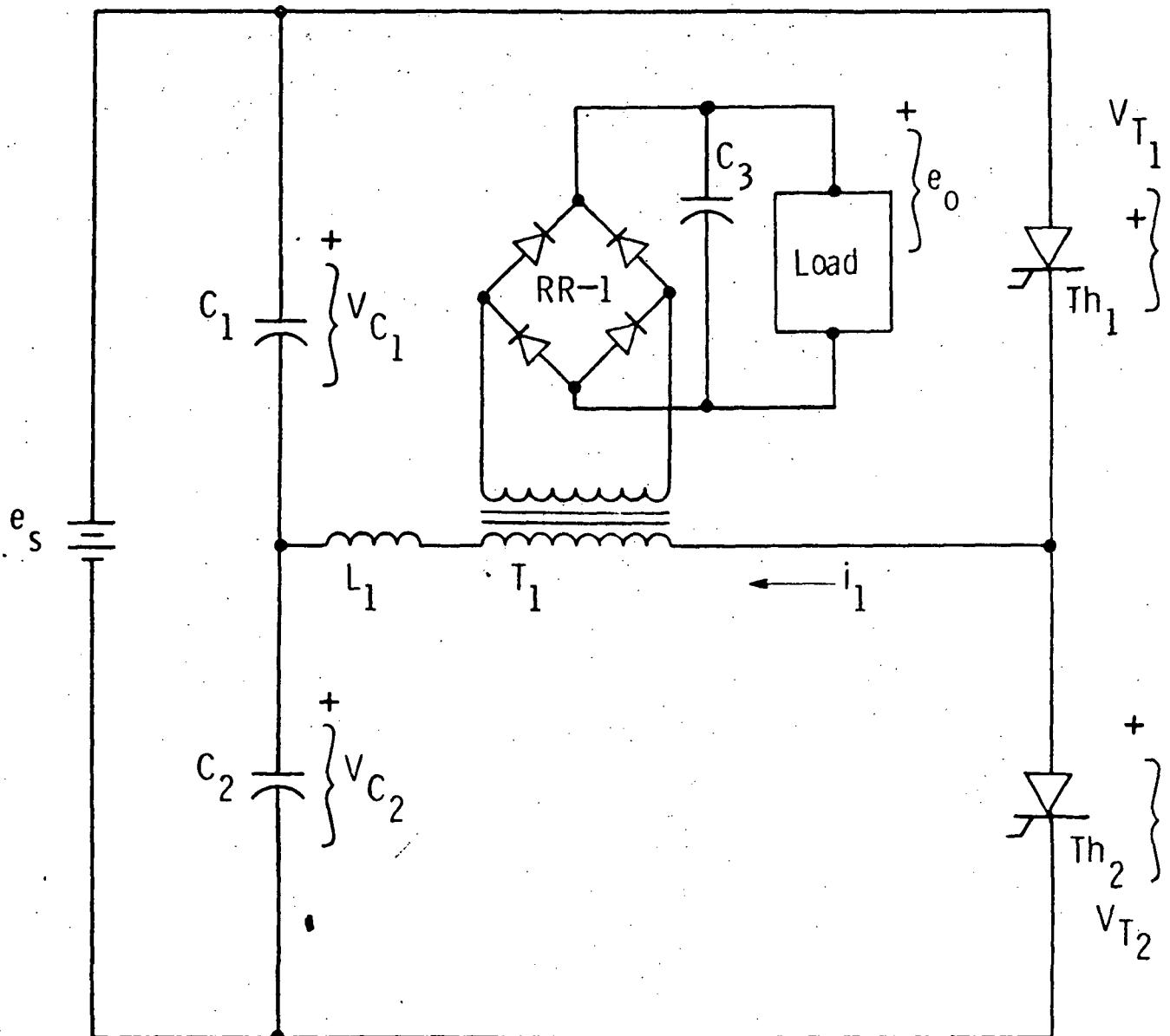
Fig. 2—Load insensitive series invertor

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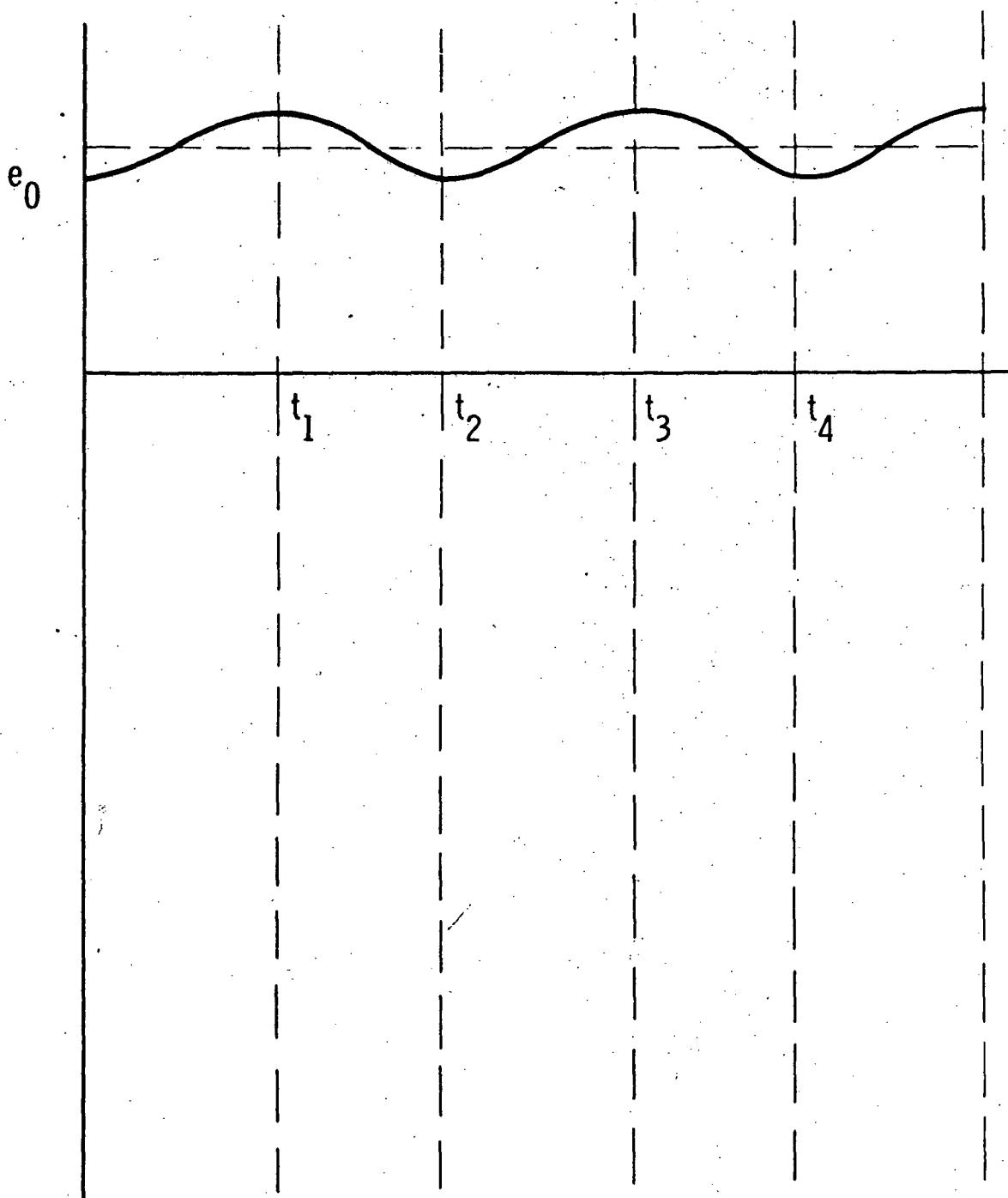
Fig. 3 —Load insensitive series invertor waveform

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The series inverter is well known for its poor regulation features when operated at a constant pulse rate. The inverter discussed in this report regulates the frequency of thyristor triggering to maintain output voltage constant. This is achieved by the standard usage of comparators, voltage controlled oscillator, and triggering systems. One other novel system of the Schwarz inverter is the use of two anti-parallel thyristors placed across inductor L_1 and transformer T_1 in such fashion as to "secure a contained excursion of the capacitor voltage waveform and an approximately constant efficiency for a given load and for variations of the same voltage e_s." The two auxiliary thyristors are triggered during conduction of a main thyristor such that main thyristor current is reduced to zero and energy stored in L_1 causes continued circulation of load current through T_1 and ultimately into the load. Discussion of the inverter control system and voltage stabilization methods are found in the literature [1,2] and are not germane to the requirements of the gate assisted thyristor. These topics will not therefore, be further amplified.

The primary interest of the gate assist thyristor development is the relationship of the GATT device performance to the requirements of the series-inverter. In general it is required that the GATT performance as a thyristor at least equate to the comparable thyristors used by Schwarz, except for recovery time. These are the thyristors spoken of with 10 μs recovery periods and which were run at 20 kHz. A one for one correspondence between standard thyristor and gate assist thyristor does not exist, although many characteristics and ratings are similar. The maximum 10 kHz operating frequency of the series inverter and the contemplated 50 kHz operating frequency demand full concurrent frequency characterization for either range. This characterization is considered outside the scope of the gate assist development and requires additional effort. Most thyristors with full frequency characterization use some form of "amplifying gate" structure to achieve fast turn-on. Full turn-on drive is supplied to annular power gates through auxiliary gates which receive drive from the anode source.

The gate assisted thyristor uses a long emitter-gate edge because of the finger emitter structure which enhances extraction of P-base charge, but which also requires a large drive for effective turn-on. Since drive to the long emitter periphery does not originate with the anode as with the amplifying gate, high drive for effective turn-on must be supplied from the actual gate of the gate assist thyristors. This is as large as a 15A pulse.

Another feature of gate-assist thyristor which alters normal thyristor performance is the lack of gate emitter shunts which are used to obtain high dv/dt rating. Since these shunts would simply act to bypass gate assist drive, making the gate assist process more difficult, shunts are not used. While gate assist performance is helped, transient susceptibility deteriorates. However, the effect of gate-emitter shunts may be obtained if the devices are always operated with an external bias resistor combination between gate and emitter such that dv/dt ratings in excess of 400 V/μs are obtained. The bias source voltage is always less than the gate emitter avalanche voltage and losses due to the bias are small.

Several parameters of the GATT switch bear inter-related characteristics which should be understood when testing and applying these units. The characteristics reflect the normal design trade-offs required to product a gate-assist switch. As an example, latching currents for gate-assist units could be as high as six amperes. In general, units optimized for turn-off will sacrifice some switching performance. Hence, the current level at which the sum of the alphas equals one could be much higher than the normal thyristor. As a consequence, other performance is influenced by this feature. Minimum gate voltage (V_{GT}) and gate current (I_{GT}) to cause turn-on or firing are impeded by high latching current. If a gate-assist device with a minimal gate drive and high latching current is tested at current levels below the latching current, there may result a condition in which the device is

forward biased but not truly switched; yet a high anode voltage and relatively high anode current of several amperes may exist in the device. Such testing has frequently resulted in catastrophic failure due to the high dissipative nature of the combination of conditions extant. As a result, the characteristics of V_{GT} and I_{GT} are normally not tested for this device. Latching currents are also measured at anode voltage levels no higher than 25 volts to avoid excessive dissipation if the latching current is high. If operation is required at current levels below the latching current level, a continuous drive of at least one-quarter of the latching current level must be supplied.

1.3 The Thyristor and the Gate Assisted Thyristor

In the above type of circuit, the thyristor is always at a disadvantage when compared with a device with gate control. To obtain a short turn-off time with a thyristor, the stored charge must be swept out by the application of a large reverse bias voltage with the accompanying flow of reverse current. The circuit under consideration does not provide the required reverse voltage, with the result that the thyristor turn-off times realized are long. When a GATT device is used, however, reverse gate current is applied during the interval $0 \leq t \leq t_1$ as defined in Figure 6, when anode voltage is essentially zero. As a result of this current, some of the charge stored in the device is swept out. The remaining charge is swept out when forward anode voltage is reapplied, but at this time, sweep-out takes place in the presence of the flow of reverse gate current, which is the normal condition of operation of a GATT. As a result, the GATT operates in its normal mode in this circuit and optimum performance is obtained, as opposed to use of even the fast-switching thyristor, which is not operated in optimum fashion by this circuit and yields nonoptimum performance. The only circuit change necessary for use of the GATT will be the inclusion of a reverse bias gate pulse generator that will apply reverse bias to each GATT following anode current commutation.

1.4 The Gate Assisted, Fast Turn-Off Thyristor Switch

The circuit requirements of a typical series inverter circuit as discussed in Section 1.2 can be summarized in the two major specifications, namely, the recovery time and the rate of reapplied forward blocking voltage. Very few, if any, commercially available 50A fast turn-off thyristors have turn-off times less than 10 μs, when the rate of reapplication of voltage is 50 or 100 V/μs. At a 400 V/μs rate of reapplied voltage, their turn-off times become much longer. The design of a specially constructed thyristor was therefore necessary. This section describes the objectives and the direction of the design philosophy which achieved them, while the next section delineates the testing goals.

1.4.1 Design Objectives and Philosophies

The objectives for the GATT device are given in Table 1. Certain parameters usually given in thyristor specifications, holding current, gate current to fire, gate voltage to fire, and turn-off time with anode voltage are missing from the list because of their limited meaning in the context of a GATT type of device. The limitations are in part theoretical, and in part practical, as will now be shown.

Four-layer pnpn switches are commonly discussed in terms of their two-transistor analogs, which involves an npn and a pnp transistor combined.
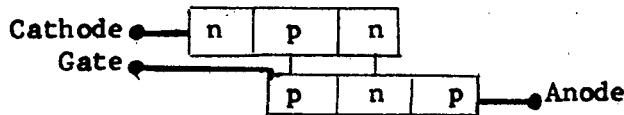
From this model, the static forward voltage blocking characteristic, V_{BO}, is developed as is the V_{CEO} of a transistor, and depends upon the anode current I_A, as

$$I_A = \frac{\alpha_{pnp} I_g + I_{CBO}^{pnp} + I_{CBO}^{pnp}}{1 - \alpha_{npn} - \alpha_{pnp}} \tag{1}$$

Table 1 -- Design Objectives for the GATT Devices

PARAMETER		SYMBOL	VALUE
Maximum Forward Blocking Voltage	Volts	V_{FB}	600
Maximum Reverse Blocking Voltage	Volts	V_{RB}	600
Maximum Forward Drop at $I_A = 50$ A	Volts	V_F	2.0
Maximum Junction Temperature	°C	T_j	125°
Maximum Crest Anode Current	Amps	I_A	50
Recovery Time (See Fig. 4) after $I_A = 50A$ is circuit commutated off	μs	t_r	2
Maximum Initial Rate of Reapplied Voltage Rise , Exponential to V_{FB} Maximum, at $T_j = 100$°C	V/μs	dV_{RM}/dt	400
Maximum Rate of Current Removal	A/μs	di/dt	10

In this model, and even in more realistic extensions, the separate α's, or common base current gains of the separate component transistors figure very prominently. Switching of the thyristor into the on state occurs when the α's sum to unity, or greater.

$$\alpha_{npn} + \alpha_{pnp} \geq 1 \qquad (2)$$

Once switched on, the pnpn device will remain on so long as equation 2 is satisfied.

Design of a thyristor for specific applications entails proper selection of the geometrics and resistivities to specify αnpn and αpnp for the characteristics desired. Thyristors of "standard" design typically involve $\alpha npn \cong 10 \; \alpha pnp$ at the switching point. The α's are current dependent, as is the case in any transistor, and gate turn-on triggering is accomplished by base drive of the npn transistor to raise its current level, and thereby its α to the point where equation 2 is satisfied. In the design of a gate assisted turn-off thyristor, it is equally necessary that the gate have control over the switching characteristics; therefore, the junction designs are also selected so that

$$\alpha npn > \alpha pnp$$

Fast turn-off is required of the GATT device, and to accomplish this, the units were gold-doped. By thus shortening the lifetime, the values of αnpn and αpnp at any given current level are reduced. Thus, in general, the current drive to cause switching is greater for faster turn-off device capability.

Once switched on, a thyristor will conduct until the current drive is reduced so that equation 2 is no longer satisfied. At this point, the device switches off and the minimum current required to keep it on is known as the holding current. In these fast, high power devices, the holding current is much greater than for "standard" devices, and in most cases, when we endeavored to determine its value, the devices were destroyed by a second-breakdown type of fault; i.e., as is the case

with a transistor, transit-time through the safe operating area is significant for a GATT device. The common technique for measuring holding current compares to a "dc" transient, and resulted in device destruction due to the high dissipation involved.

Similarly, efforts to determine minimum gate current and gate voltage to fire also involve operation of the device in a dissipative mode, and resulted in device destruction.

Determination of these parameters will be essential for eventual safe application of the GATT device. Since, however, their determination is frequently destructive to the device itself, they must be approached in the same fashion as are the surge current and di/dt ratings of conventional thyristors. That is, by a statistical study of a stable production line.

Determination of turn-off time with anode voltage was not made, since no application of the device is this mode was foreseen.

One final area of device design current gain, where the GATT device differs significantly from a conventional thyristor, deserves comment, and is treated below. We now define the test conditions used in device characterization.

Referring to Figure 4, the gate drive pulses are defined on the basis that the turn off is circuit-initiated, i.e., the anode voltage goes through zero. This time and rate of current removal are dependent on the components in the series inverter such as the capacitance, leakage inductance, and switching times of the diodes, etc. However, the start of current decrease can be used to trigger the assisting turn-off pulse applied to the gate. This voltage has a minimal source impedance; thus the voltage will not exceed the breakdown voltage of the gate-cathode junction throughout the entire t_w period.

V_{FB} (max)

(a)

V_F

0

dv/dt

t_r t_v

I_A

$-di/dt$

(b)

t

t_d

V_g max

t_w

(c)

$-V_g$ max

$-I_g$

(d)
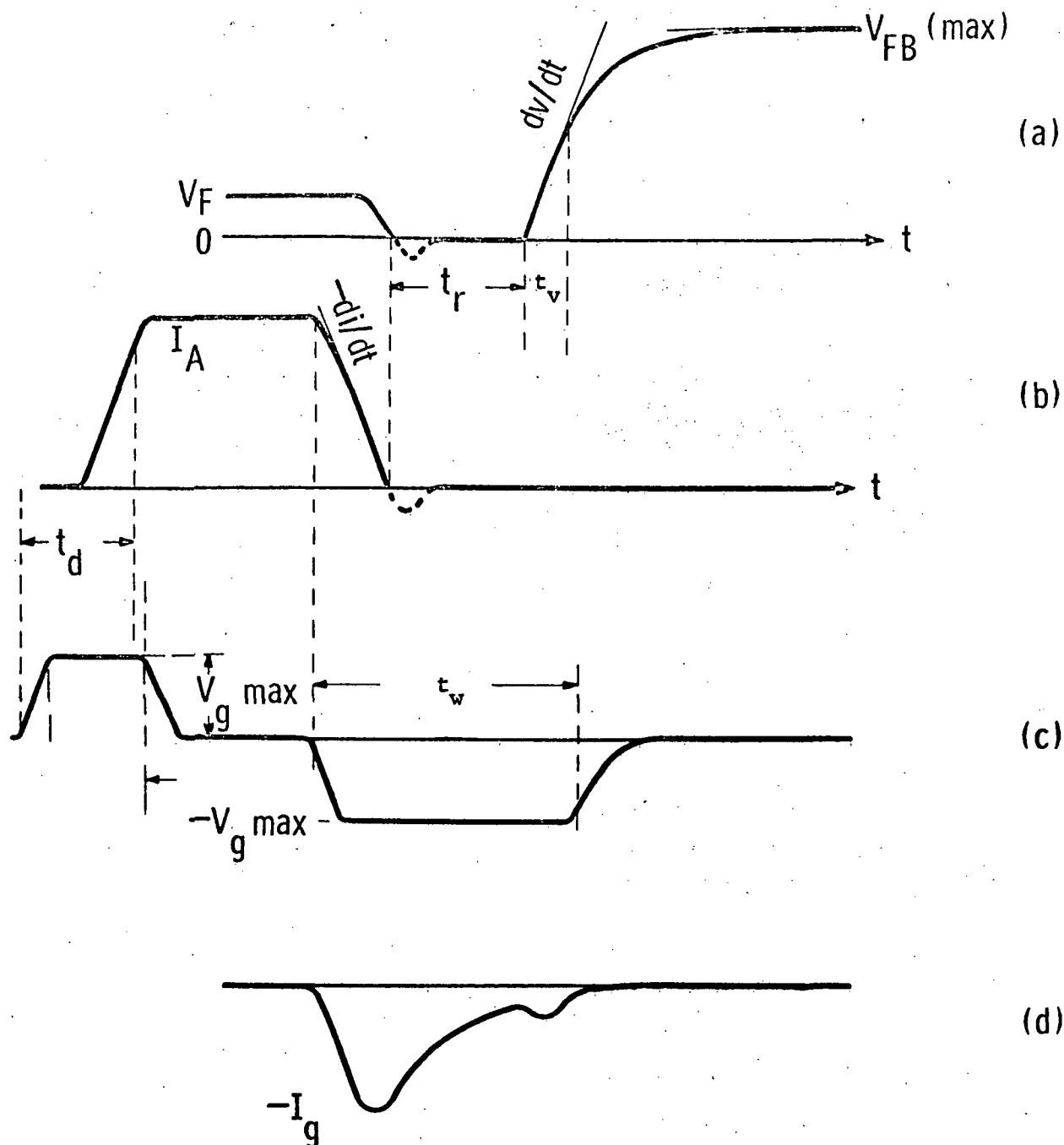
Figure 4 — Nomenclature for turn-off waveform.

a) Anode Cathode Voltage

b) Anode Current

c) Gate Cathode Voltage

d) Gate Current

The t_w is the time in which the assisting gate pulse must be applied; not only will it extract the remaining stored charges, it should also remove the d (CV)/dt current when the forward blocking voltage is re-applied. The gate current is really a dependent variable since the magnitude of the current is controlled by the available charges from the device. Thus the gate current will reach a peak and will decrease as the charge supply dwindles. For this reason, we do not use as a criterion the ratio of steady maximum anode current to instantaneous peak gate reverse current, I_A/I_G, which is commonly and misleadingly called "turn-off gain".

1.4.2 Device Design Consideration

The turn-off limitations of conventional thyristors are due mainly to the residual stored charge in the device. If this charge can be removed more rapidly through the application of a supplementary drive signal to the gate, the delay time before the forward blocking voltage can be reapplied is significantly reduced.

Function of Gate Control

The conventional thyristor is a regenerative device; its gate is used to initiate cathode injection, which in turn causes anode injection. This action continues as regenerative feedback to drive its blocking junction into deep saturation for forward conduction. The gate loses its control once the regeneration takes effect. After the area adjacent to the gate is triggered "on", while the more remote regions are still blocking, some lateral flow of current will occur. This divergence of the current flow provides the required triggering current for its neighboring area to trigger it on. The "on" region thus spreads out to cover the whole junction area, permitting the device to carry hundreds of amperes. The spreading mechanism has been experimentally verified and its velocity determined for certain types of construction.[4-7]

This mechanism superficially gives an extremely high "turn-on gain" of a thyristor and is generally independent of its maximum current capability.

In a filamentary section of PNPN where lateral spreading is not a factor, although the gate is not needed to keep the device in conduction due to its internal regenerative feedback, it is possible to draw enough current out of the gate to disrupt its regenerative cycle and to return it to the blocking or "off" state. In the same way, the gate of a thyristor can be reverse-biased to prevent it from injecting charge carriers or to remove excess carriers due to regeneration at high temperatures or to remove $d(CV)/dt$ current, especially when dv/dt is high.

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The last stated characteristics are compatible with series inverters. However, in a high current, large area device where the current spreading feature is used, only a small area surrounding the gate electrode can be effectively controlled. The limitation is due to lateral voltage drop in the gate.

Lateral Voltage Drop

If the device is already turned off, the application of forward blocking voltage V_{FB} will cause the space charge region to widen toward a new equilibrium value. In doing so, it develops a current $d(CV)/dt$ uniformly over the whole area. This current is in a sense equivalent to a positive gate current in the P-base region with no external gate connection. Now if a reverse bias is present prior to the application of V_{FB}, the cathode-gate junction may be already cut off (depending on $-di/dt$), and there can be no injection from the cathode. With this reverse gate voltage, the current $d(CV)/dt$ or the displacement charge $d(CV)$, will be swept toward the gate electrode. The P-base region, however, has a certain resistivity due to its level of doping. If a unit length of this section is considered and if b is a point where the voltage drop is zero (Figure 5), the voltage drop V_{go} at the edge is

$$V_{go} = \frac{Rb^2}{2} \frac{d(CV)}{dt} \qquad (1)$$

If the gate drive voltage V_g is greater than V_{go}, the x = b point will shift further from the gate into the cathode area to increase the distance b so that $V_{go} = V_g$. More gate current will be drawn since total I_g is proportional to b.

However, the displacement current in the region x > b cannot be swept out. In that area, the cathode junction is thus forward biased and may permit the device to turn on. In other words, the gate has no control over this area.

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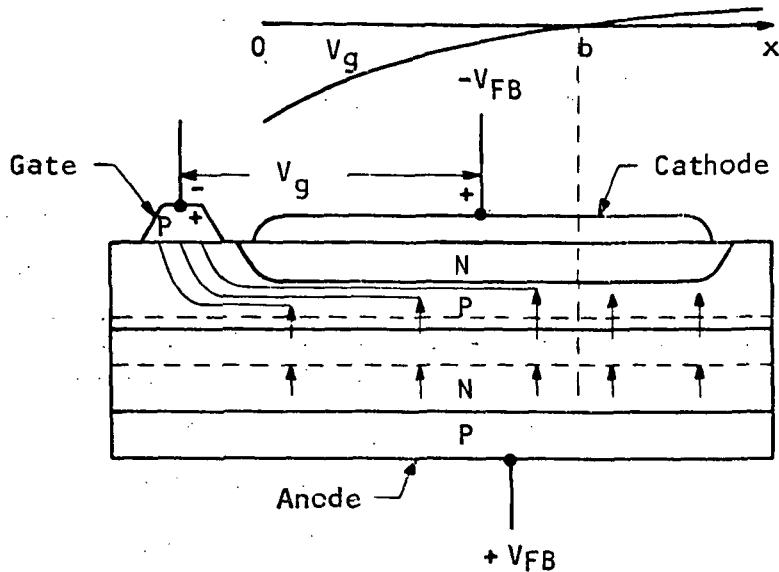
Figure 5 — Lateral voltage drop under the cathode.

It is obvious that higher negative gate voltages can control larger cathode areas. However, the quadratic relationship soon will demand voltages at $x = 0$ greater than the breakdown voltage of the cathode gate junction.

Since the breakdown voltage and the P-base resistivity ρ are usually fixed for a thyristor, the most profitable approach to render full gate control is to make the cathode in narrow strips with the gate surrounding it. The width of the strip can be easily calculated from Equation 1 and the doping profile.

In conclusion, the basic requirement for the gate to maintain control of a large area device is to use long and narrow cathode emitters. This is the essence of the GATT device. The maximum utilization of these and the electrical contact that permits uniform distribution of gate current have been central to this contract.

Removal of Stored Charges

In the foregoing discussion, we have assumed that the circuit commutation is fully effective. In other words, the cathode junction is blocking and gate assistance is to draw out the $d(CV)/dt$ current. However, if the circuit voltage and current merely drop to zero without effective reverse sweeping of the excess charges in the device, the gate may function differently.

Using the charge control approximation, the switching characteristics in general have been calculated (References 6 and 7). Similarly, the charge distribution under our specific conditions can be illustrated. Figure 6 shows the charge decay without gate control: Fig. 6a shows the effect of forced commutation with reverse sweep-out current; Figure 6b shows the natural commutation turn-off as current decreases to zero. With the gate drive and natural commutation, the turn-off is shown in Figure 7a. If reverse drive is available then the residual charge can be reduced even faster. The excess charge left in the base region will determine the time when the fast dv/dt can be reapplied. For this reason, the dotted line in Figure 4b indicates that a circuit arrangement which would allow some reverse current may be desirable.

1.5 Statement of Work

These are the broad philosophies of thyristor design which we believe to be consistent with the meeting of the objective specifications: a 600-volt, 50-amp thyristor which will recover in $2\mu s$ in the face of a reapplied dv/dt of $400V/\mu s$ after conducting with a 2-volt forward drop. Two major portions of the work on this contract were aimed at the implementation of these design philosophies and the delivery of 10 or more thyristors meeting the specifications. A third task was the development of test circuitry to verify the specifications, to simulate the use of these devices in the series inverter. Finally, it was expected that the
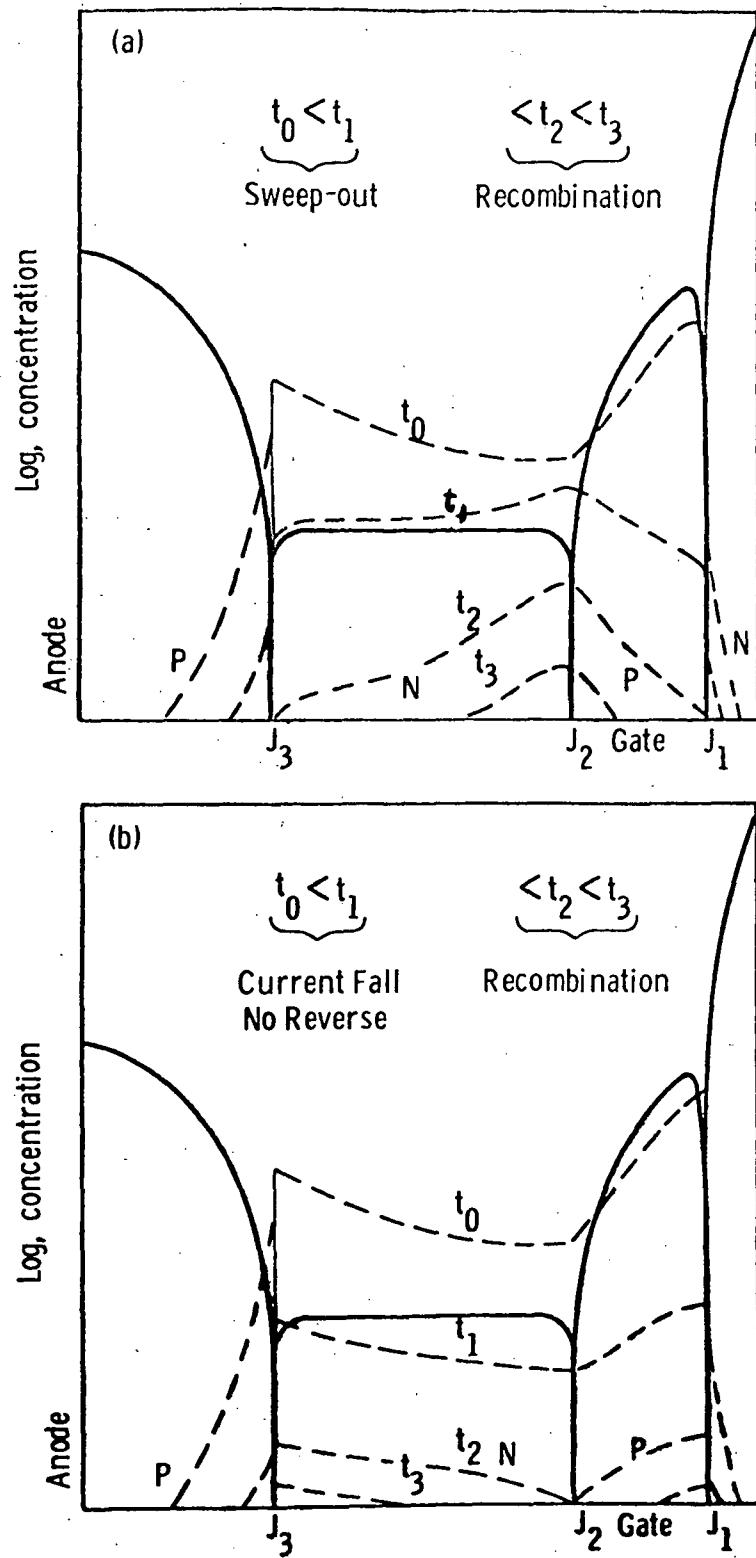
Figure 6 — (a) Sweep-out with reverse current and decay of charges.
(b) Current fall without reverse sweep-out and blocking recovery.
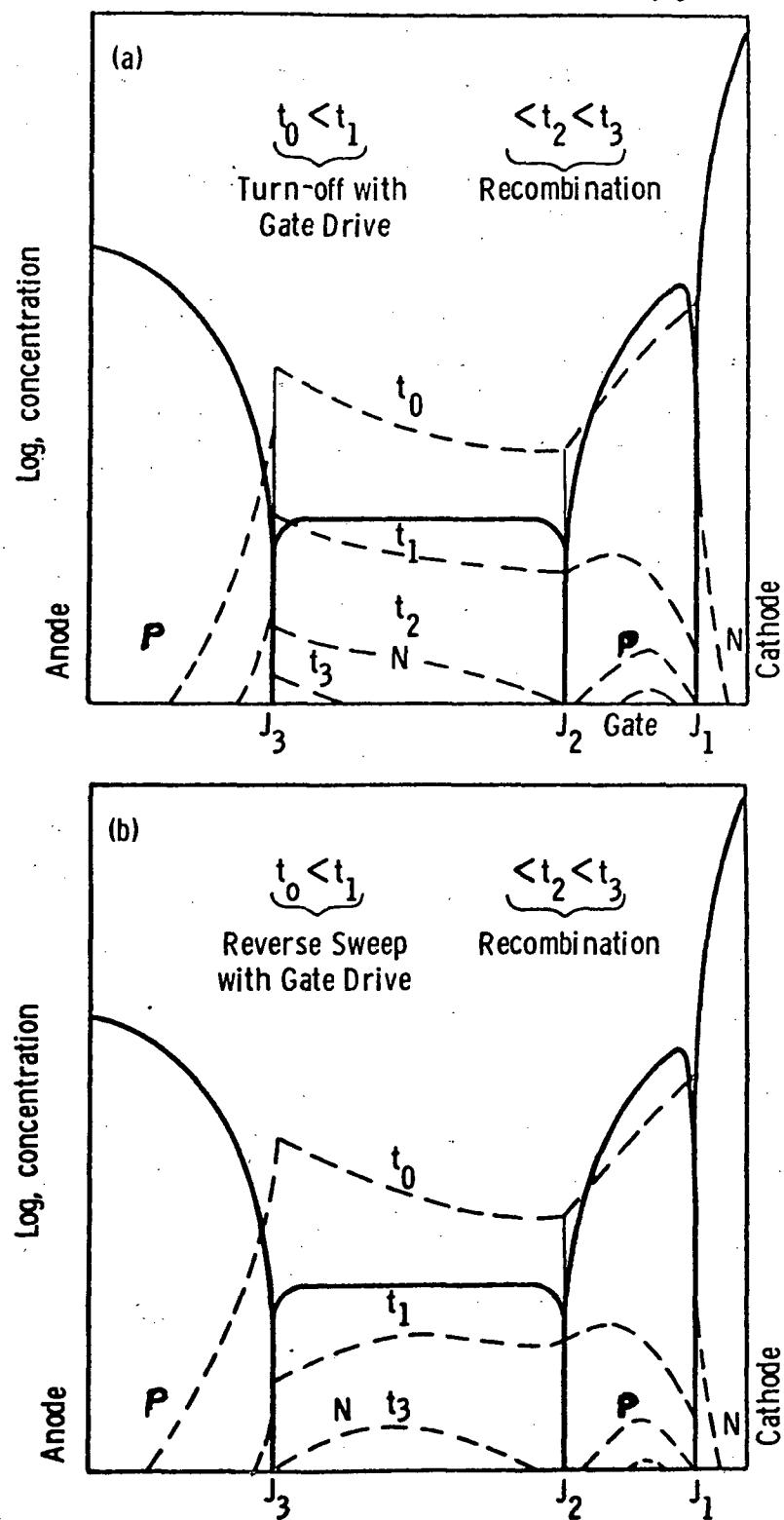
Figure 7 — (a) Current fall with gate drive. (b) Reverse sweep-out with gate drive.

performance of the contract would lead to a deeper understanding of the developments required to improve the switch beyond its present ratings, to higher voltages, higher currents, shorter recovery times and lower forward drops.

Westinghouse Electric Corporation has not only fulfilled but has indeed exceeded most of the objectives of this contract. GATT devices were delivered very early in the performance of the contract, devices which met the majority of the final specifications. Not only first but also second generation tests and simulation circuits have been designed and put into operation. The problem areas are now clearly defined and the potential solutions well understood.

2. PROCESSING

2.1 Introduction

GATT processing is intermediate between thyristors and transistors. The steps are related to thyristors, for the GATT unit is a four layer device, blocking voltage and handling current much like a thyristor. The steps are related to transistors, for turn-off, in current sweepout, the device is functioning in a three layer mode through the gate and emitter contacts which are interdigitated like a transistor. Much of our processing development related to the latter characteristics in particular to the nature of the fingers, the mechanical contact to them, and the ultimate capability for sweeping out stored charge. These problems were of such primary importance that a separate section is devoted to them alone. In the following, we describe the standard processing and control and some of the developments and improvements made in this. These changes are not related directly to the finger problem itself.

2.2 Standard Processing (See Figure 8)

We now outline the major process steps.

1) **Silicon** of 0.91" diameter, n-type conductivity, (111) orientation, and $10^3/cm^2$ or fewer dislocations is the starting material.

2) **P Diffusion** is effected by depositing gallium and then driving it into cleaned slices of silicon in two closed tube diffusions. Sheet resistivity and junction depths are measured after these steps.

3) **Phosphorus Deposition** is done by forming phosphorus glass on both sides of the diffused slices in a furnace from a source of ammonium phosphate maintained at 780° to 1230°C. Subsequent to this the phosphorus deposited glass is removed from the anode side by a short silicon etch. Phosphorus drive into the cathode side in an oxygen rich atmosphere provides the basic emitter region. The diffusion is slow cooled. Slices are then removed and are etched in HF to remove the oxide and glass surface layers. Sheet resistivity

- 25 -
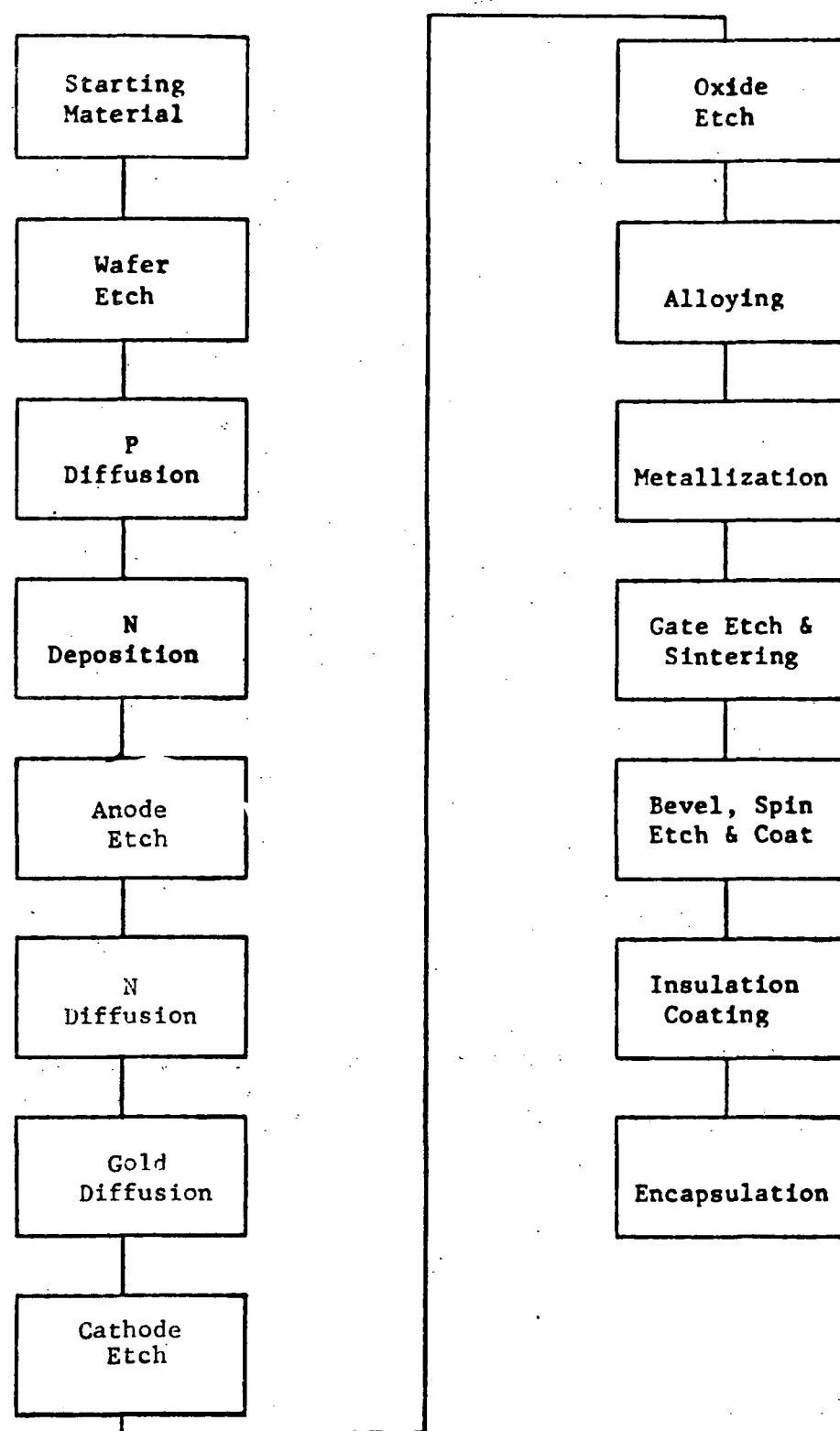
Figure 8 - Process Flow for GATT

and junction depth measurements relative to the phosphorus diffusion are made.

4) Lifetime Control is obtained by evaporation of gold on the anode side and then diffusing it into the silicon at a temperature ranging from 820 to 880°C, depending on the desired degree of lifetime reduction. Residual gold is removed and the wafers cleaned.

5) Mesa Etch of the emitter fingers is done by a long slow silicon etch, designed to maintain a flat surface while removing 15 to 18 microns of silicon. This exposes the P-gate region and defines the raised emitter fingers.

6) Alloying with a 0.94" diameter aluminum preform to a 50 mil thick moly slug of the same diameter is performed in a vacuum furnace. Subsequent to this the fusion is cleaned and aluminized by evaporation on the cathode emitter side. The metallization is photomasked and etched back to define the areas of aluminum contact. After this the aluminum is sintered above 500°C.

7) Bevel, Spin Etch, and Coat are standard thyristor operations.

8) Gate Insulation will be discussed in greater detail in the following section. The units are essentially complete at this point and may be stored, tested, etc.

9) Contacting and Encapsulation are the last operations. The proprietory Westinghouse "Compression Bonded Encapsulation" system is used as illustrated in Figure 9. In this approach a copper cathode contact is pressed on a silver foil atop the fusion which itself is resting in the package base as shown in Figure 10. The ceramic cap is welded over the top, effecting an hermetic seal. The basic design and its adaptations have been discussed at length in the final report on contract F33615-68-C-117 with the Air Force Aeropropulsion Laboratory, Wright Patterson Air Force Base, Ohio.

Ag Gate Lead

CBE Force

CBE Force

Cathode Lead Assembly:

Cu Lead

Mo Backing Disc

Ag Contact Foil

Al Metallization:
Cathode Region (typical)

Gate Region (typical)

N

P

N

P

Al Anode Contact

Mo Backing Disc

Cu Base
(Anode Lead)
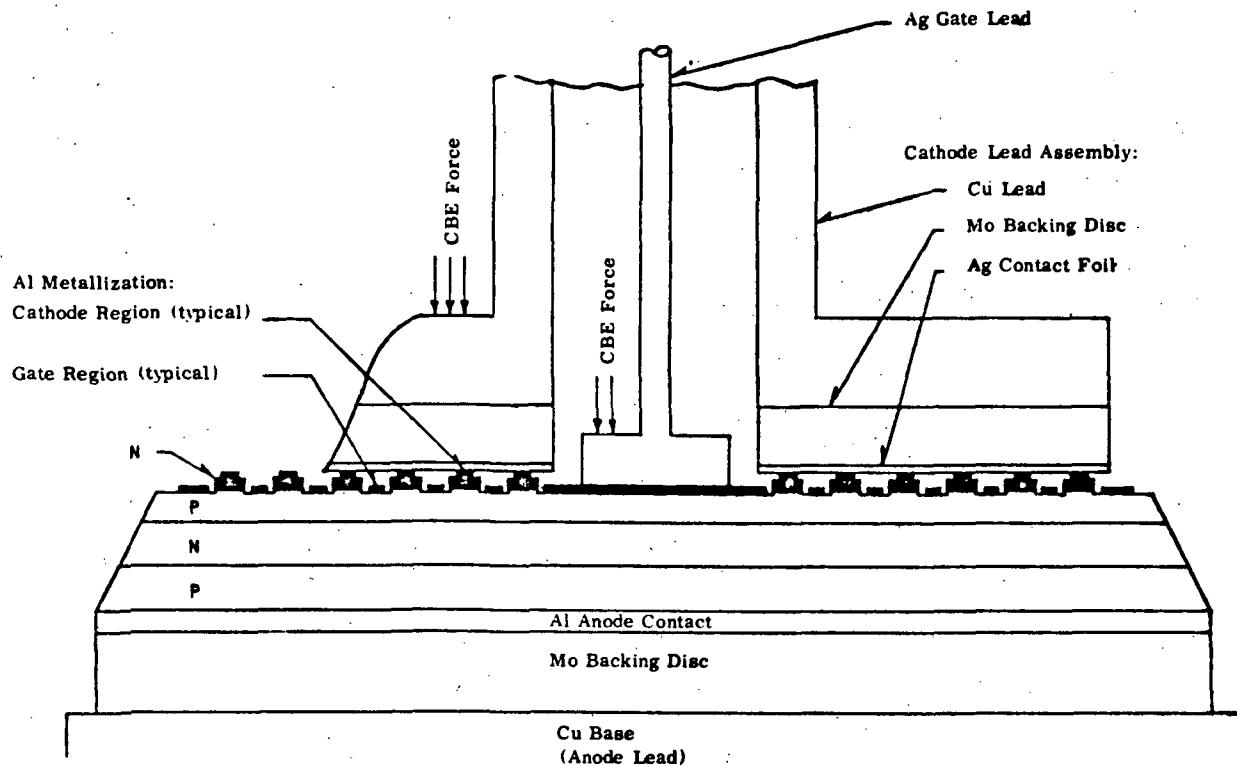
**Figure 9** — Technique used in Compression Bond Encapsulation
(CBE), an exclusive Westinghouse system.

Dwg. 859A291

Gate Lead

Cathode Assembly

Sleeving

Spring

Locator

Belleville Spring

Mica Washer

Steel Washer

Fusion Assembly

Silver Preform

Base Assembly
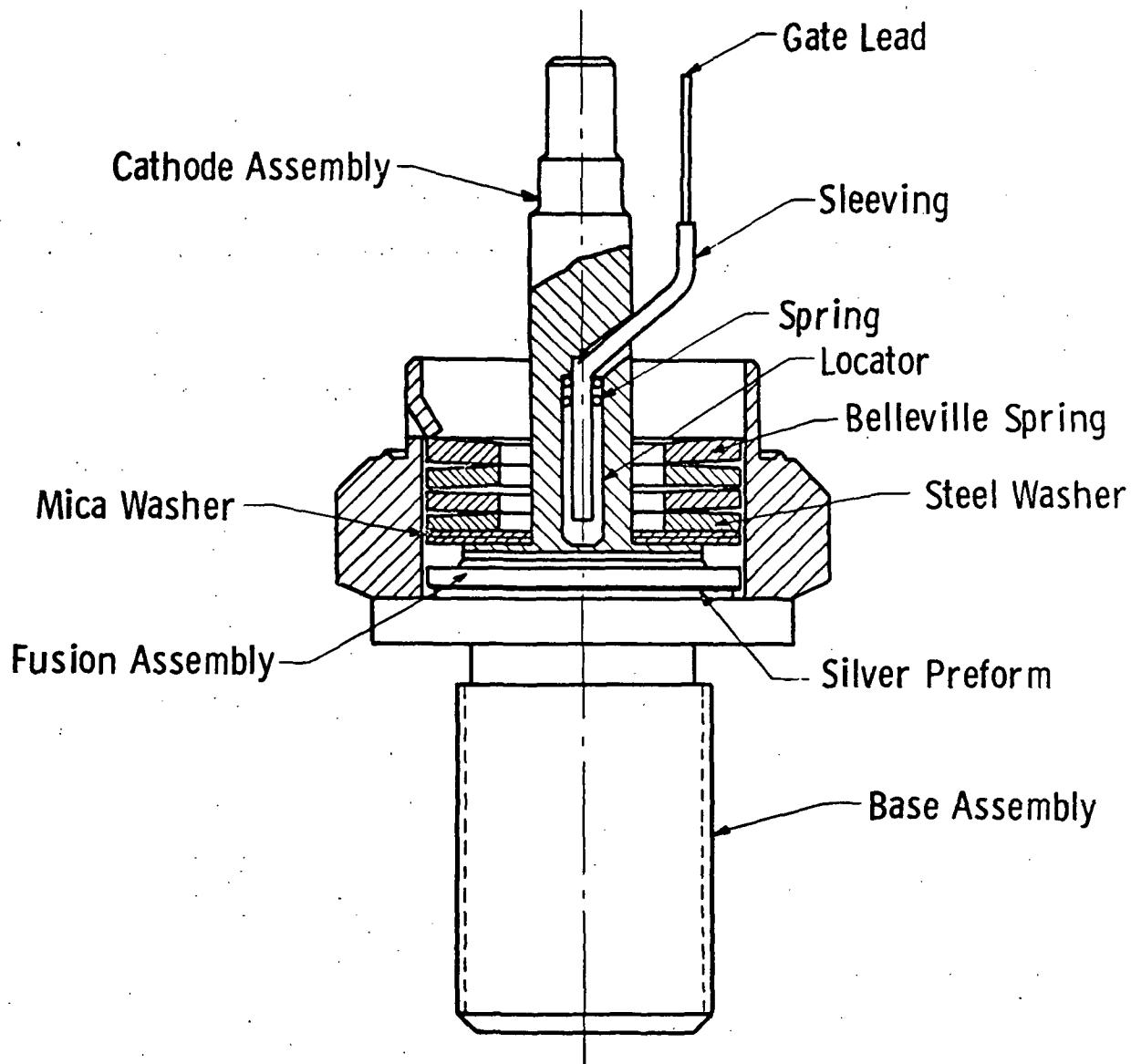
Figure 10 — Preencapsulation assembly.

2.3 Process Improvements

These are the major processing steps by which GATT devices are made. As will be discussed in the following paragraphs and in the next section, some basic alterations in the sequence were found advantageous. In addition to this, there was specific work performed on the relationship of blocking voltage and the gold doping level, on the relationship of blocking voltage and the quality of bevel lapping (a mechanical system), and on base resistivity and thickness. Of these, bevel lapping is the simplest to treat. This angle bevel is required because the junctions at the surface will have higher blocking voltage capability if they intersect the surface of the silicon at an angle other than normal. For this reason, and also to eliminate the diffused short between anode and cathode base, the silicon slice and its molybdenum backing plate are ground around the edge to an angle between 10 and 30°. We discovered during this work that the GATT slices, which are somewhat thinner than normal for thyristors because of the early gate etch, were suffering from minor cracking and breakage at the outer edge of the silicon molybdenum junction. Blocking voltage suffered. A better quality lapping machine was found and when this was used, average blocking voltages increased by approximately 200 volts.

2.4 Blocking Voltages

The degree of lifetime reduction by gold diffusion, the P base resistivity and thickness relate directly to the blocking capability. This is particularly true of V_{RB} and its dependence on junction operating temperature. When gold is present, higher generation currents are required and the internal or bulk leakage of the device at a given temperature is in general higher than its counterpart without gold. These leakage currents rise exponentially with temperature. Thus if one specifies a safe current level and uses this to define a blocking voltage, then this blocking voltage will be relatively constant up to that junction temperature at which the exponential rise in leakage suddenly becomes apparent. Above that temperature, the blocking voltage must of necessity decrease sharply. Figure 11 shows this dependence for three devices, one from run 52B and two from run 52C.
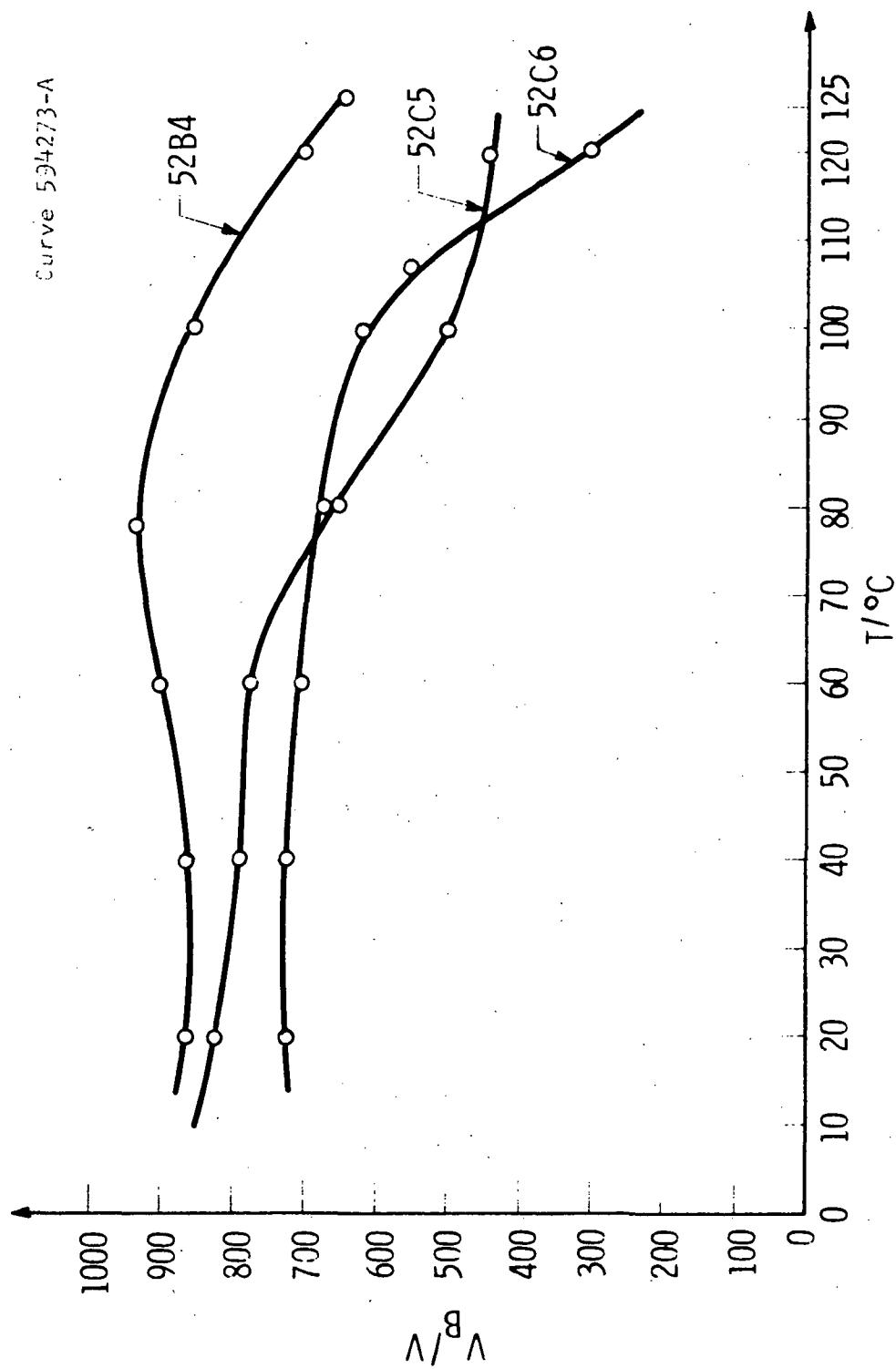
Fig. II — Blocking voltage versus temperature for 600 V GATTS

These devices differed primarily in their p-base width, as can be seen from Figures 12a and 12b. The differences are shown in Table 2 and also in the resistivity profiles in Figure 13 and 14.

The crucial point is the expected and good correlation between the p-base width and the blocking ability. Run 52B has the wider base width and clearly blocks higher voltages at all temperatures and especially at 125°C. Run 52B4 with its 46 micron base width is capable of withstanding well in excess of 600 volts in the reverse direction at all temperatures whereas 52C5 and 52C6, at 37 microns, are at best 450 volts at T_j = 125°C. Overall, the characteristics in Figure 11 are typical of GATT devices and are consistent with the dependency generally reported in the literature for gold doped thyristors. The most notable departure is the lower temperature of the breakpoint. For GATT devices this is about 80°C while for thyristors generally, with their lower level of gold, the breakpoint is usually somewhat higher, perhaps 110°C or 120°C. The GATT devices in general require the higher level of gold responsible for this difference to improve their recovery. With this exception we have found the blocking voltage trade-offs in GATT devices closely parallel those for thyristors generally. GATT devices have no unusual traits in this respect.

Table 2 - Design Differences Between 52B and 52C

	W_B (μm)	ρ_p (ohm-cm)	N^+ (cm^{-3})	ρ_N (ohm-cm)
52B	46	0.1	10^{20}	60
52C	37	0.1	10^{20}	34
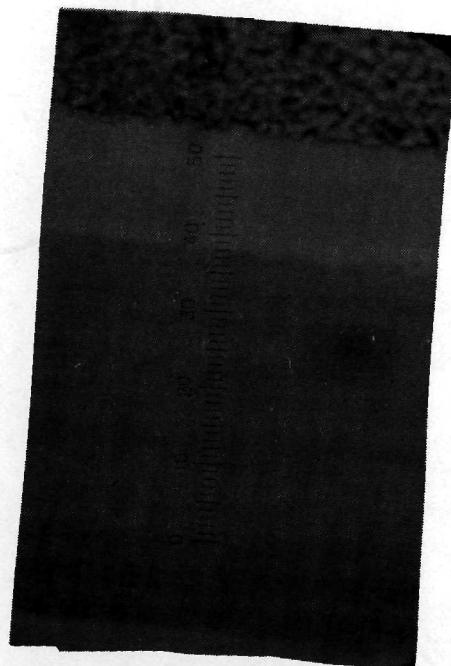
Aluminization

W_n 13.9μ

W_p 46.5μ

Figure 12A.   52B
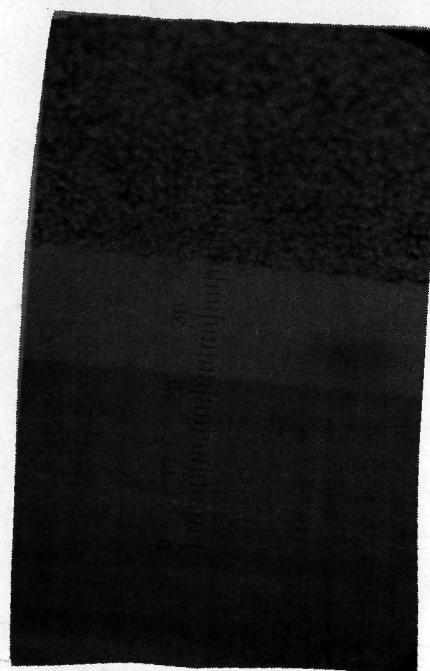
Aluminization

W_n 13.9μ

W_p 37.4μ

Figure 12B.   52C
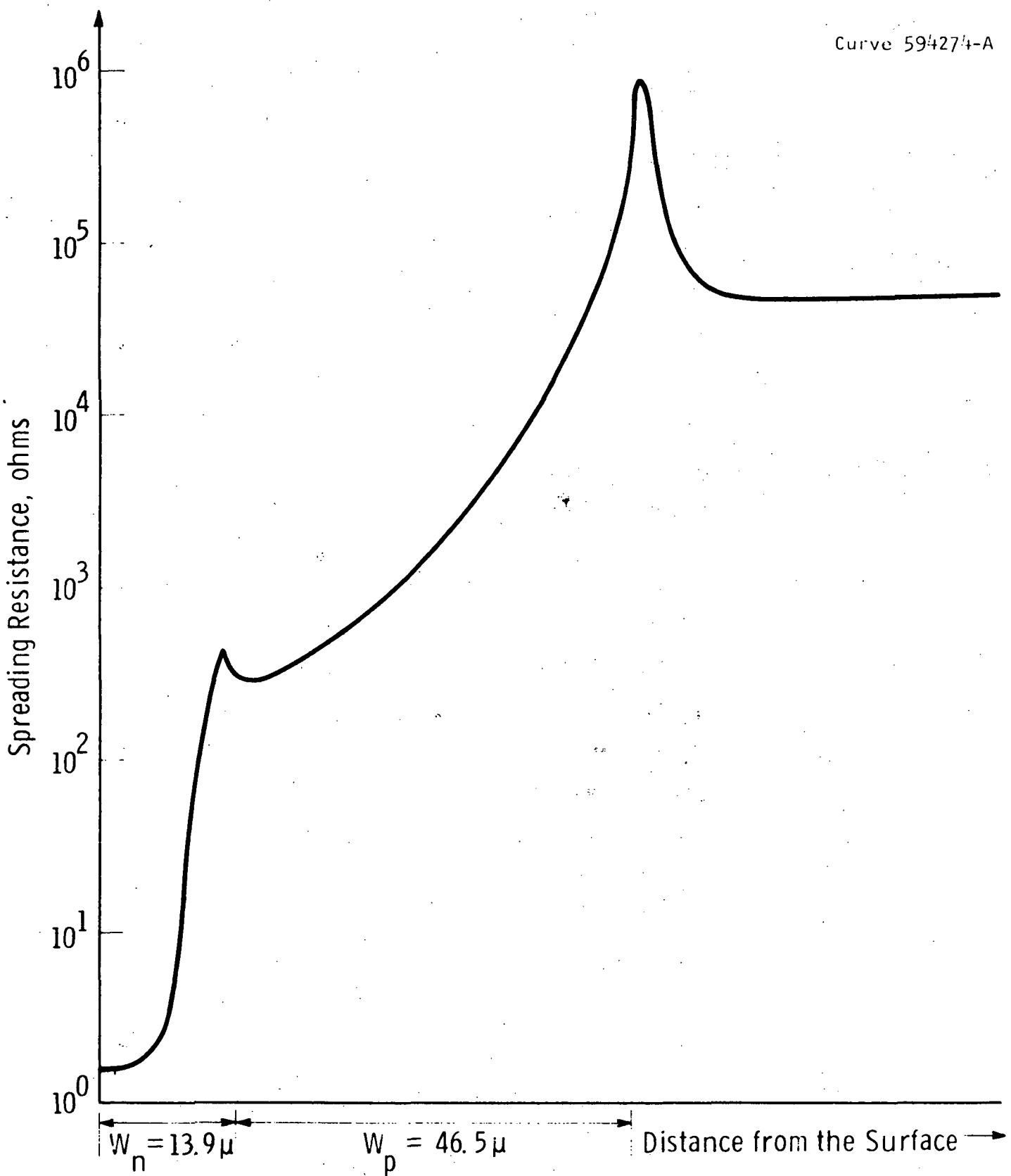
Fig. **13** —Diffusion profile of Run 52B
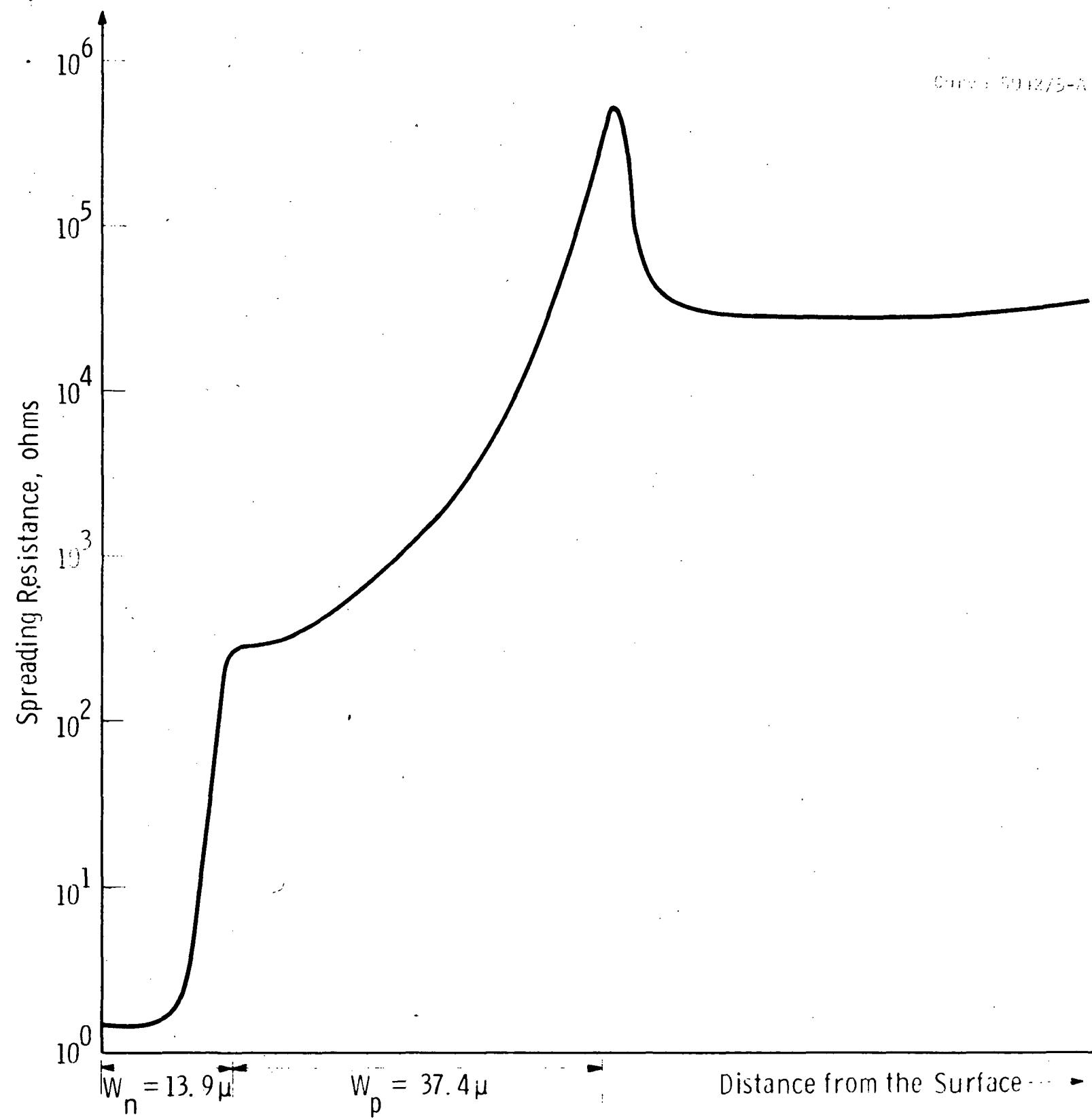
Fig. 14—Diffusion profile of Run 52C

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3. CHARGE EXTRACTION AND GATE-EMITTER CHARACTERISTICS

3.1 Introduction

To extract charge from the commutating device, the gate emitter junction must be driven towards and even through its avalanche voltage. The gate surrounds the emitter fingers and extracts charge from underneath the emitter contact area, thus allowing this junction to recover. Except for this mechanism, recovery of the device and its ability to face re-applied dv/dt would be determined primarily by carrier lifetime. Since lifetime has already been reduced considerably by the gold diffusion, charge extraction through the gate becomes the vital difference between the GATT device and a conventional thyristor. The GATT device differs also from the transistor in that removal of the latter's base drive is sufficient to cause it to drop out of conduction. GATT devices do not do this. Therefore, considerable time and effort has been spent upon improving the efficiency of charge extraction and in understanding the mechanisms that govern it so that the maximum rates are obtained.

If the gate emitter junction is leaky, then not all the gate current drawn is residual stored charge and higher gate drives will be necessary to accelerate commutation. We early observed that many encapsulated devices had soft avalanche characteristics and leakages in the order of several amperes, a current that is substantial when compared to the extracted charge. Under these circumstances, much of the gate drive signal is diverted into ohmic losses. Examination of individual devices soon revealed that although the reverse leakages of most of the thirty-six individual emitter fingers were excellent, there were a few with disastrously high leakages, 100 milliamps or even one ampere. Such leaky fingers are very prone to turn-on failure which will occur when dv/dt is reapplied.

Simultaneously, an investigation of the peak currents achievable from back biasing individual non-leaky fingers, as a measure of charge extraction, was performed. It revealed that there was a parallel variation in this capability. Some fingers extracted charge notably better than others. We discuss the leakage situation first.

3.2 Gate-Emitter Leakage

Recognition of gate emitter leakage as an individual finger problem rather than a distributive one, led to the examination of the steps in processing where fingers might degrade. We found that immediately following etching of the emitter finger mesas, the leakages were low and uniform in the order of microamperes. On the other hand, prior to encapsulation the leakages were variable and some were in the ampere range. For example, twelve wafers alloyed to molybdenum would reach the finger test out of 25 starts. In one particularly good run, one unit of the twelve had four fingers with leakages so high that they could be considered shorted; the remainder had microamp leakages. Two units had one finger each shorted, the balance exhibiting virtually no leakage. Two additional units had one finger each which measured leakages in the milliampere range, the balance good. All fingers of the seven remaining wafers had leakages in the microamp range. Thus we are speaking of a total of eight fingers, half of which are completely inoperable. Thus, although the yield to microampere leakage on a device (or wafer) basis is less than 50%, the yield on a finger basis is very high.

Typical data for a single wafer is shown in Table 3. I_{gt} at V_{BR} = 12.5V is shown for the eighteen shorter fingers first and then for the eighteen longer ones. The leakages range from 0.5 ma to 0.18 amperes, with one shorted finger. Excepting this one, all could be made to turn off individually, although the device could not function properly as a unit. By both following material forward through the line and working backward from encapsulation, we pinpointed two sources of degradation. The first was the physical handling of the fusion after finger etch. We demonstrated that once the bare junction is exposed, it is extremely vulnerable to physical damage. In the initial process sequence this junction was unprotected during alloying and bevel lap operations. Specifically, the surface was exposed to powdered graphite and an abrasive lapping compound in these steps. Elsewhere, experiments showed that handling with steel tweezers and even plastic ones,

Table 3--Variability in Emitter Finger
Characteristics on a Typical Wafer.
Throughout, I_A=10A, V_{BR}=12.5V and I_g=3.5A.

SHORT FINGERS				LONG FINGERS			
Finger Number	t_s μs	t_f μs	I_{gt} in mA @ V_{BR}	Finger Number	t_s μs	t_f μs	I_{gt} in mA @ V_{BR}
1	0.8	1.0	0.5	1	1.0	3.5	50
2	1.0	1.0	45	2	1.5	2.5	20
3	1.0	2.0	20	3	1.0	2.0	30
4	0.8	3.0	12.5	4	1.0	5.0	20
5	1.0	1.8	12.5	5	1.0	11.0	20
6	1.0	2.0	12	6	1.0	9.0	10
7	1.0	2.4	12.5	7		shorted	
8	1.0	5.5	30	8	1.0	4.0	10
9	1.0	5.5	17	9	1.0	3.0	150
10	1.0	5.0	150	10	1.5	1.0	120
11	1.0	4.5	90	11	1.5	2.5	120
12	1.0	0.5	40	12	1.5	0.8	120
13	1.0	1.5	150	13	1.0	2.0	35
14	1.0	2.0	125	14	1.0	2.0	100
15	1.0	0.5	85	15	1.0	1.5	100
16	1.0	0.6	24	16	1.0	1.5	10
17	1.0	1.0	17	17	1.0	1.0	10
18	1.0	1.0	8.5	18	1.0	1.2	35

caused an immediate increase in leakage. Even touching the unit with a cotton swab wet with distilled water was sufficient to cause short term degradation of gate-emitter characteristics.

Further experimentation established the second source of junction leakage. It was found to be introduced during the final aluminum evaporation of the top contacts. In this step, the entire upper surface of the wafer is covered with aluminum. A subsequent photomasking operation protects the contact areas and allows a selective etch to be used to remove the unwanted metal which lay across the exposed junction. A minor improvement came when it was realized that faulty instructions to the operator were causing him to evaporate with a substrate temperature well in excess of 300°C. Such substrate heat is routinely used for cleaning in the vacuum system prior to evaporation; but, if applied during evaporation it causes appreciable micro-alloying to occur. Alloying at the exposed junction would obviously result in high reverse leakages. But elimination of this error was insufficient to yield devices with a 100% yield of perfect fingers. It was concluded that either the aluminum itself or sodium contamination in the metal was still contributing to surface states and leakage.

These observations suggested four courses of action.
1. Reschedule the mesa etch so that the fingers are exposed as late in the process as possible.
2. Rework the handling procedures so that there is no physical contact with the gate-emitter junction after exposure.
3. Institute a program to recover the junctions that have failed.
4. Protect the junction throughout.

3.2.1 Rescheduling of Process

In Figure 8 and in Section 2.2 we outlined the initial process schedule for GATT devices. The first attempt to reschedule the mesa etch was to do it after the alloying step. When this was done, finger leakages improved but not as dramatically as we had hoped. However, this had an unanticipated side benefit. The incidence of silicon cracking during the brazing of the wafer to the molybdenum substrate was reduced. Previously, the etched wafer frequently shattered; presumably because it had been thinned some10% by the mesa etch.

3.2.2 Physical Handling

The handling of conventional thyristors, with broad area emitters and short emitter periphery is generally not critical insofar as casual contact with gloves and the like to the top surface. These devices only become sensitive after the final etch of the junction bevel and prior to coating; and this interval is short. The GATT device on the other hand has a very long emitter periphery. A major effort was made, therefore, to eliminate any handling operations which might lead to contact with the bare junction. The devices are only picked up by their edges and no materials are allowed to come in contact with the top surface. The processing is done exclusively by solution, with liquid contact, and agitation is restricted to ultrasonics or a mild agitation by moving the wafers about in the bath while retained in their rack. Photoresist is removed entirely by non-mechanical means. The testing of individual fingers for leakage is done by a contact applied from above rather than using, e.g., the original sliding contact on a spinning fixture.

3.2.3 Junction Rework

Since these programs did not fully achieve uniformly low leakage in all fingers, a set of experiments was carried out to determine if the junctions could be recovered after damage. It should be possible to eliminate the leakage caused by physical damage with straightforward silicon etches. This was indeed easy to do. Despite this, it was not possible to obtain a high yield of devices in which there were no fingers of abnormal leakage. Thus, the problem area was narrowed and defined, and a partial solution obtained. The conclusions led inescapably to the need for a better protection scheme for a junction, a passivation that could be put on the device early to maintain the low leakages observed immediately after emitter finger etching. We discuss this program in the following section.

3.2.4 Emitter Gate Passivation

Four kinds of coatings for passivation against junction degradation were tried.

1. Photoresist
2. Thermally-grown SiO_2
3. Chemically vapor-deposited SiO_2 with boron or phosphorus additions
4. Chemically vapor-deposited SiO_2/Si_3N4 films

Photoresist - The simplest protection of all is a layer of photoresist. It can be put down exactly where required, it adheres well and has moderately good long-term stability. Its advantages clearly outweigh other choices such as silicones or paralyene. The reverse of the aluminum contact etch back mask is used and photoresist is laid down with this. The insulating resist thus covers the exposed junction. Since photoresist does not withstand a vacuum environment well. it could only be used after the aluminum contact had been laid down and etched back. Thus the junction was protected only in contacting and packaging. Although the photoresist may have been successful, it obviously could not eliminate leaky finger generation during the metallization itself. Unfortunately at the time photoresist was tried, the seriousness of degradation in metallization was not known so that the outcome of the photoresist experiments could not have been anticipated.

Thermally-Grown SiO_2 - The easiest inorganic passivation attainable on silicon is a thermally-grown oxide. For GATT devices, this coating was established following the mesa etching of the fingers and the removal, also by etching, of the temporary etch mask. Exposure of the bare wafers to an oxidizing atmosphere at moderately high temperatures permitted conversion of the silicon at the device surfaces into a passivating SiO_2 film. Since this film covered the entire surface, a photomasking step followed by etching in buffered HF was necessary to remove the SiO_2 from the gate and emitter contact areas. Aluminum evaporation was then carried out as before. However, no perfect devices were obtained either because the conditions of growth of the thermal oxide were to severe for the device doping or because the thermal oxide was too thin to withstand the attack of the aluminum during metallization.

<u>Chemically Vapor-Deposited SiO$_2$</u> - To avoid
changes in dopant concentration and distribution during the consumptive
growth of oxide films on the silicon surfaces, attention was given to
chemically vapor-deposited (CVD) films. Many systems have been proposed
for this purpose, but the most promising for low temperature application
is the oxidation of silane gas, SiH$_4$, with oxygen. When combined directly,
these gases react in the gas phase to form an undesirable smoke; but when
diluted, the reaction will occur almost exclusively at the surface of a
hot object exposed to the gas stream. Accepted practice calls for the
dilution and thorough mixing of both the oxygen and silane gas streams
with argon or nitrogen before the two reactants are even brought together.

Typical values of concentrations and flow rates
for a quartz tube reactor with a 2 inch x 6 inch cross section are:

Dilutant (carrier) gas: dry N$_2$

Total gas flow: 40 l/min.

Silane flow (3-5% in Ar): 10 cc/min.

Oxygen flow (20 times silane flow): 200 cc/min.

Substrate temperature: 350-400°C

Given these conditions, deposition rates of 400-500Å/min. can be expected
with little or no vapor phase reaction.

Since pure SiO$_2$ deposited this way is not as
chemically resistant or as well matched to silicon in thermal expansion
coefficient as is thermally grown SiO$_2$, a borosilicate glass film was
also tried. The borate glasses generally are low fusing, fluid glasses
which can be densified at the low CVD temperatures. The well-known
optimum concentration of 22% B$_2$O$_3$ in the film was obtained, using es-
sentially the same conditions as listed above, but oxidizing a mixture
of SiH$_4$ and B$_2$H$_6$ in which the diborane made up 26% of the reactant gases.

An additional dopant gas, PH$_3$, was also used.
The objective was to use a phosphorus doped SiO$_2$ to provide gettering of
sodium and other metal ions which are known to degrade device characteristics.
Again, conditions were essentially as above except that the reactant gas
in the stream included 5% phosphine.

All of these deposited films were laid down
over the entire wafer and, as was the case with the thermally grown
oxide films, were etched to expose the contact areas prior to met-
allization. A further similarity with thermal oxide passivation was
the exposure of the CVD films to attack by aluminum during metallization
and sintering. In view of the latter, it is not too surprising that
here, as before, no devices with a complete set of perfect fingers were
obtained. Overall yield was, however, substantially improved.

Silicon Dioxide/Silicon Nitride (Oxide-Nitride)

Passivation - A process similar to but somewhat more complex than the
formation of CVD oxides has been developed at the Westinghouse Research
and Development Center. Like the oxidation of silane, oxide-nitride
passivation or ONP, does not consume any of the substrate surface. The
silane gas is reacted first with oxygen, then later with ammonia and
finally once again with oxygen to form a three-layered coating. A
notable difference is the higher temperature ($> 700°C$) required for ONP.
Because all the layers are applied in the same reactor without inter-
mediate handling, the process is only a little more complex and certainly
does not reflect the complexity of the deposit itself.

The functions of the various layers are briefly:

a) SiO_2 to provide a good interface between the passivating
film and the device surface;

b) Si_3N_4 as a highly impervious barrier to sodium and heavy
metal ion contamination and further to provide some gettering
action for these ions; furthermore it is not attacked by
aluminum which is a great advantage;

c) SiO_2 as an etch mask for the Si_3N_4 film.

The usefulness of SiO_2 as an etch mask comes about
because it can be photomasked and etched using conventional techniques
and reagents. Si_3N_4 is not attacked by these reagents. On the other hand,
Si_3N_4 is attacked by hot phosphoric acid which has little effect on SiO_2.
The cover oxide layer can therefore be masked and etched using buffered HF
to expose areas of Si_3N_4. Subsequently, phosphoric acid is used to etch
the nitride. Once windows have been opened this way in the Si_3N_4 film,
dipping the wafer in buffered HF a second time then provides access to

the silicon contact areas through the underlying oxide film, while the unetched nitride layer in its turn serves as an etch mask.

The work on oxide-nitride passivation included two variations of silicon dioxide-silicon nitride layered structures. In one, undoped SiO_2 was chemically vapor deposited on the silicon surface followed by Si_3N_4 and an undoped SiO_2 top layer. In the other variation the structure was the same except that the first SiO_2 layer was doped with 5% P_2O_5 by the addition of PH_3 to the chemical vapor deposition gas stream. Both procedures followed these steps:

a) Prepare the basic alloyed unit by the standard techniques; i.e., gallium, phosphorous, and gold diffusions, alloying to a moly base with aluminum and etching the fingers by photomasking techniques.

b) Deposit about 1500A U. of SiO_2 by chemical vapor deposition, adding PH_3 to the gas stream if phosphorous is desired in the oxide.

c) Deposit a like amount of Si_3N_4 by chemical vapor deposition.

d) Deposit undoped SiO_2 as in Step 2 as a capping layer.

e) Photomask and etch the top SiO_2 layer in standard buffered HF etch. Remove the photoresist.

f) Etch the Si_3N_4 in boiling H_3PO_4 using the top SiO_2 pattern as a mask.

g) Etch the underlying oxide layer (the top layer of SiO_2 is also removed).

h) Continue with the normal fabrication procedure.

The process sequence in which the application of the coating is done after alloying, definitely is undesirable. The unit is heated to 700°C during the original alloying step, at which temperature the molten alloy must be confined mechanically to keep it from running out of the joint. When the unit is reheated for the Si_3N_4 deposition, run-out occurs leaving the silicon only partially supported. During subsequent bevel lapping for blocking junction isolation, the unsupported regions crack and break off, destroying the unit.

A further alloying problem was also discovered. On otherwise good units, regions of anomalously deep penetration of the alloy-silicon interface were noted. The interface was not flat or mildly undulating as desired but consisted rather of mesa-like structures projecting into the silicon. These structures could degrade reverse blocking voltage by causing premature punch-through of the depletion region; in the worst case they could cause anode to cathode shorts. Tentatively, the location of these regions has been attributed to the effects of sand-blasting the backs of the wafers before and after gold diffusion. They are probably the result of local wetting and temperature gradient zone melting.

3.3 The Limits Of Charge Extraction

Although the ultimate capability of a GATT device is the sum of the individual static capabilities of the 36 fingers, the present performance is not since dynamic effects predominate. Examination of the dynamics of individual finger charge sweep-out capability is clearly a part of the requirements of this contract. Two parameters of individual fingers are of interest. The first is the recovery time, which consists of storage and fall time; and the second is the peak current capability in commutation.

Table 3 shows measurements of the individual short and long fingers of a typical wafer taken at a constant peak anode current of ten amperes with $I_G = 3.5A$, and $V_{BR} = 12.5V$. (Note that this anode current corresponds to a total device current density of 360A). The scatter amongst storage times is low. The start of charge sweep-out is thus relatively constant across the entire wafer which speaks well for the uniformity of processing. It is not surprising that the storage times are slightly longer for the second group of fingers, for they are physically longer in the actual pattern. The fall times on the other hand scatter widely. Again, there is an indication, albeit weak, that the fall times of the longer fingers are longer; at least the longest fall times 11 and 9 µs, occur in this group. The values range from these highs down to a low of half a microsecond. Those slower fingers determine the time of application and rate of rise of reapplied voltage. The slow fingers are last to sweep out charge, the last to recover, and hence are most prone to dv_{rm}/dt failure. If a slow fall time should also happen to be coincident with a high gate emitter leakage, these difficulties would undoubtedly be compounded.

Table 4 shows the maximum sweep-out capability of a group od eight adjacent fingers on a particular wafer. To obtain these data, the anode current through a given finger was steadily increased until it reached that level at which destructive failure was thought to be imminent.

Table 4—Maximum Turn-off Capability of Eight Fingers on a Single Wafer. The parameters shown are all taken at the limiting current.

Finger Number	t_s μs	t_f μs	I_{gt} off A	I_{ato} A	V_f V	V_g V
1	2	4	6	30	5	
2	2	5	5.5	26	5	15
3	1	7	5.5	20	3.5	16
4	1	6	11	22	3.5	24
5	2	4	6.5	30	4.5	15
6	3	3.5	6	30	4.0	15
7	2	5.0	6.5	30	4.0	16
8	2	6.5	8.0	32	4.0	20

The anode current may or may not develop a small tail prior to failure, and if this is observed, the device must be shut down. But failure is difficult to anticipate and the margin before destruction is small. For this reason it has been difficult to obtain this data on a large number of fingers or on large numbers of devices.

The peak current varies from 22 to 32 amperes. Other wafers in which fewer fingers were tested have shown that some exceptional fingers can handle as much as 40 amperes. Since there are 36 fingers on each wafer, it would seem that the current handling capability of each alone is more than adequate for the GATT application. Dynamic problems during switch-off must be minimized. The data in Tables 3 and 4 again confirm the basic premise that a finger selection scheme was an appropriate engineering solution to improve quickly GATT performance. The observation on leaky fingers led to the same conclusion. These two facts, coupled with our knowledge of the current extraction capabilities in the fingers of a related device, the gate controlled switch, demanded that selective finger contacting be used in GATT devices to improve performance.

Several schemes have been used to selectively contact the better fingers and to leave out the poorer ones. All are based upon the bonding of a wire along the length of each good emitter finger. The CBE cathode pressing down from above then contacts only the wired fingers.

The first technique used short lengths of wire, approximately two millimeters long, thermal compression bonded to the outer end of each good finger. The remainder and middle of the device was covered with a mica washer slightly thinner than the diameter of the wires. This washer supported much of the mechanical load from the cathode, avoiding severe deformation of the wires. It was observed however that the cold flow in the wires was sufficient that the load on these became marginally low, especially when the device was thermally cycled. Then differential thermal expansion around paralleled structural paths in the package caused some of

The cathode-wire contacts to open intermittently. Overall device characteristics were not stable.

The final solution was to eliminate the mica washer altogether and to carry the full compression bonding load on 15 mil diameter silver wires running the entire length of each emitter finger. Many devices have been packaged this way and no indication of instability, either electrical or mechanical, has been observed. Wire bonding is an expensive operation however. Not only must the fingers be individually tested and marked, the wires must be individually tested and marked, the wires must be laid onto the emitter contact with considerable precision. When they are not, the wire swages over the edge of the junction and shorts out the gate. Thus we have a good engineering solution based upon a poor manufacturing technique.

4. TESTING

4.1 Introduction

The gate assisted turn-off thyristor has been conceived as a thyristor with gate control qualities used to hasten the turn-off time associated with normal thyristor commutation. As a consequence, all the evaluation parameters of the GATT device are normal thyristor ones except where the new functions of gate control must be defined. Thus we have in this section first an outline of the standard thyristor testing procedures used to characterize the more normal properties of the GATT device. These include, for example, forward and reverse blocking voltage, the forward drop, as well as a number of other useful parameters, many of which were not specified as the targets for this contract. Secondly, we have the dynamic evaluation of GATT performance which has of course been influenced by the desired utilization of the device as a fast thyristor for use in the high frequency series inverter. Thus properties like the turn-on time, the recovery time, the rates of re-application of voltage, and finally the overall dynamic gate characteristics had to be determined. Two circuits have been used for this. The first is the simulator specified in the work statement. The second is a more recent and far more interesting system suggested by Drs. F. Schwarz and C. Renton and designed specifically to test the recovery time and dv_{rm}/dt characteristics most stringently. We outline both.

Throughout this section test data will be given on particular devices which represented the current product at the time the tests were done. We have chosen to segregate the collection of final characteristic of the delivered devices (as well as some data on certain intermediate groups) to Section 5. Thus the purpose of this section is to outline the testing procedures rather than to evaluate the collected characteristics of all the completed GATT devices.

4.2 Static Characteristics

4.2.1 Forward Blocking Voltages - Devices with avalanche
values in excess of 600V have been routinely fabricated, albeit with
low yield. As had been described in the processing section, the GATT
devices exhibit some downgrading of forward blocking ability with in-
creasing temperatures. This is related primarily to the presence of
gold in the device. In general the reverse blocking voltages are lower
than the forwards, possibly because the gold is diffused from the anode
side and hence is more concentrated at the reverse blocking junction. In
some devices the blocking voltage may be increased by shunting the gate-
cathode with resistance, or shunting the gate-cathode with a resistance
in series with a negative bias. Because of the large distributed gate
area, resistance shunting alone has only little effect upon increasing
forward blocking voltage. The latter method of applying ten ohms in
series with ten volts across the gate cathode will increase forward
blocking voltage capability by five or ten percent. In some instances,
limitation of forward blocking ability is caused by surface leakage
effects, for which bias changes from gate to cathode will have no effect.

As with thyristors, forward blocking ability is defined as
the blocking voltage existing at prescribed forward leakage current, at
specified junction temperature. The forward blocking specification is
as follows:

$$V_{FB} = 600 \text{ volts at } I_F = 15 \text{ ma, } T_{CASE} = 125°C$$

$$10 \text{ ohms, } -10 \text{ volts gate to cathode}$$

4.2.2 Reverse Blocking Voltage - Reverse blocking abilities
of the order of 600 volts have been produced. The reverse blocking
specification is as follows:

$$V_{RB} = 600 \text{ volts at } I_F = 15 \text{ ma, } T_{CASE} = 125°C$$

4.2.3 <u>Reverse Gate Voltage Measurement</u> - The gate-cathode
characteristics of the GATT behave as a forward biased junction in the
forward direction and a reverse biased junction when the gate is forced
negative. See Figures 15a and 15b. The forward characteristic of
Figure 15 suggests the absence of gate-cathode shunt paths which are
normally used with all diffused thyristors to increase dv/dt. The GATT
does not use gate-cathode shunts (shorted emitter construction) in
order to keep the turn-off effectiveness of the gate at its maximum
capability. If shorted emitters were used, turn-off drive would be
diverted from the gate-base area and be bypassed by the shorts. This
is illustrated schematically in Figure 16.

Gate shunts are used with thyristors to divert current caused
by transient anode voltage from the thyristor gate. This desensitizes
the gate, and increases the device dv/dt rating. Figure 15b and Figure 17
show the reverse gate characteristics of two different devices, the first
of which is low leakage, and the second higher gate-cathode leakage. For
device 52A7 the indicated leakage path was unintentional and only sub-
tracts from device performance. The gate assisted switch is designed
without gate-cathode shunts, and those with lowest leakage such as the
device of Figure 15b are considered the highest quality units.

Besides the obvious reason of diverting turn-off current, other
reasons exist for avoiding GATT devices with high gate leakage. When
reverse voltage is applied to the device of Figure 15b, voltage from
13-14 volts may be supported by the gate with little current drain where-
as the unit of Figure 17 requires a current of 150 milliamperes be
supplied when -14 volts is applied to the gate. The leakage currents
of some GATT devices have been as high as 1-5 amperes, and this places
a high strain on the turn-on and turn-off gate circuitry. The un-
necessary leakage current requires a larger gate power source, greater
losses in gate drive circuitry, and more expensive components. As a
consequence it is easier to drive a gate assisted thyristor if the gate
shunt paths are minimized.

DEVICE #52B14
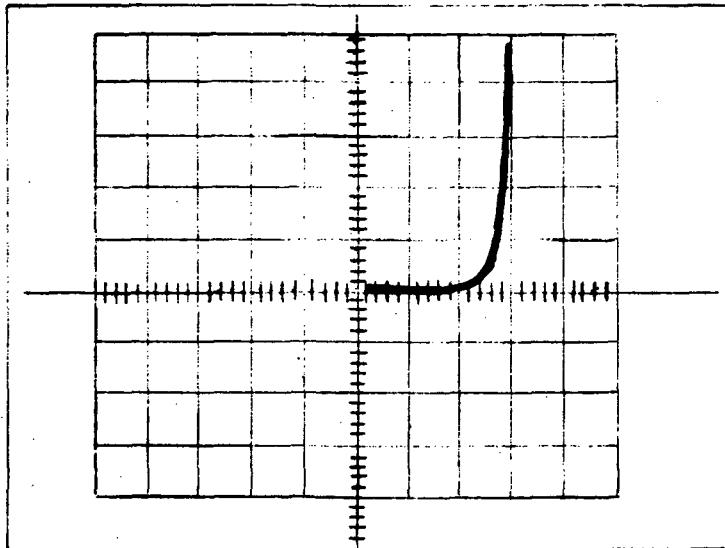
Hor.   .2V/div
Vert. 5ma/div

Fig. 15a. Gate Cathode V-I (Forward)

DEVICE #52B14
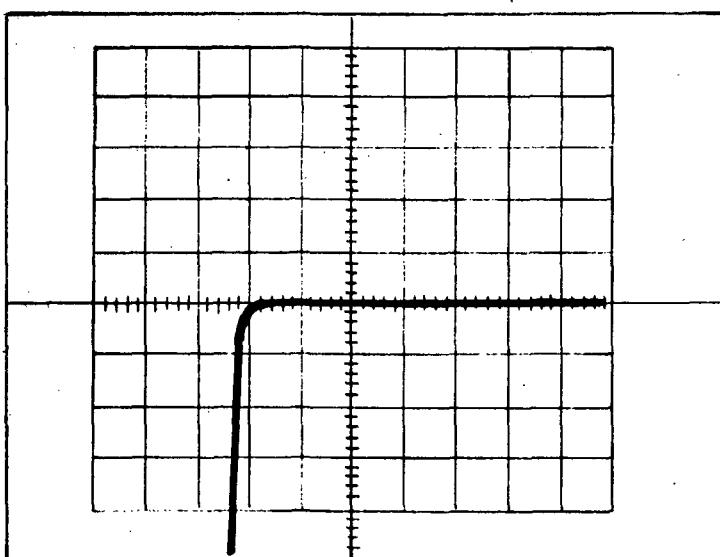
Hor.   2V/div
Vert. 5ma/div

Fig. 15b. Gate Cathode V-I (Reverse)
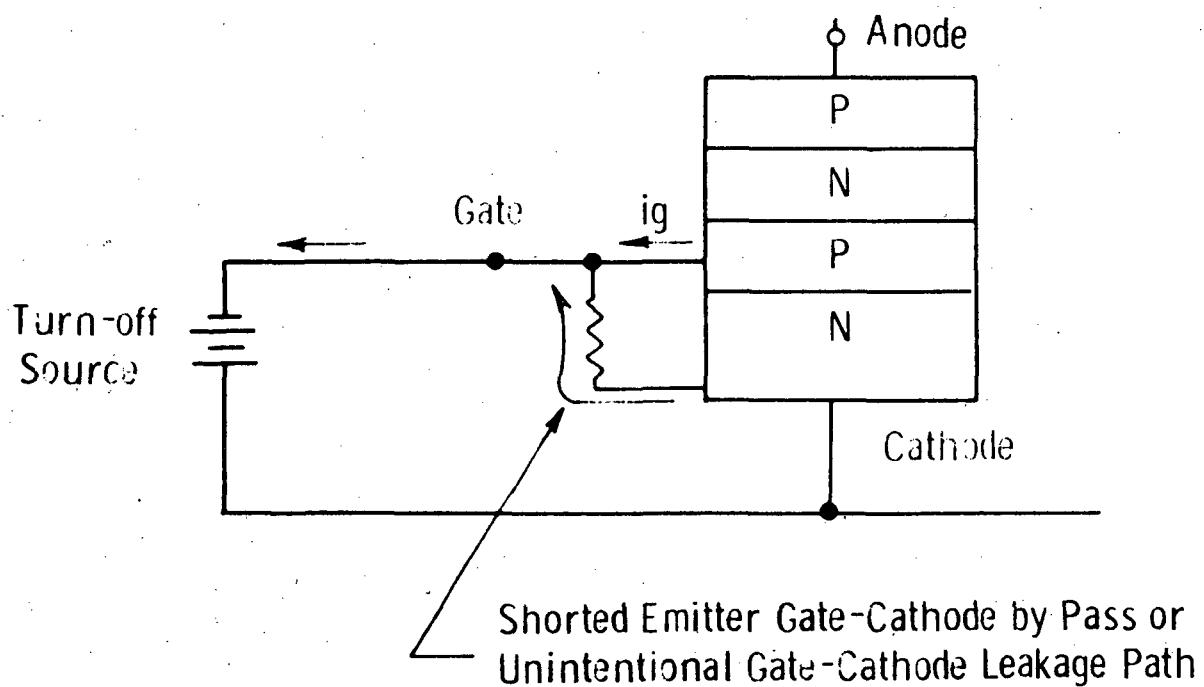
Fig. 16 Equivalent gate leakage resistance

DEVICE #52A7
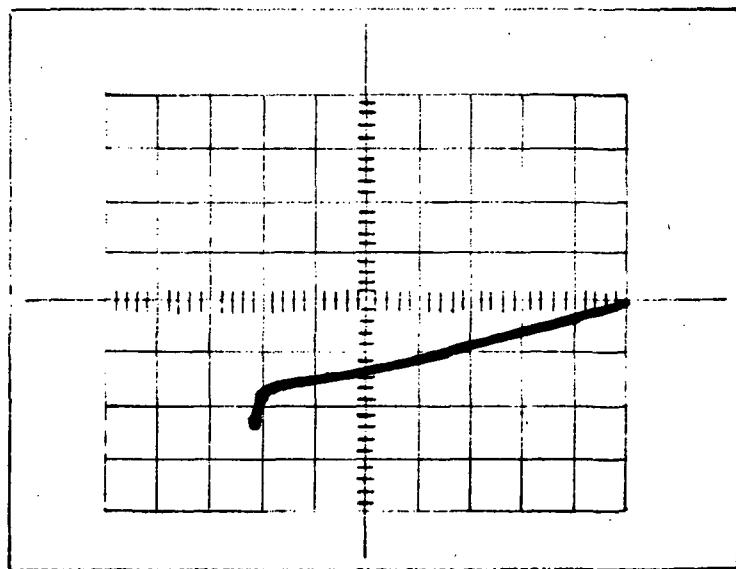
Hor.   2V/div
Vert. 100 ma/div

Fig. 17. Gate Cathode V-I (Reverse)

Reverse gate voltages were measured on GCS-type devices produced in a parallel program in Westinghouse. These ranged from -10 volts to -18 volts. Since no shunts are used with this device either (structurally it is equivalent to the GATT device), a nominal bias is applied for all measurements and operating circumstances. The bias consists of -10 volts in series with 10 ohms applied from gate to cathode of the switch. Without bias the device shows a dv/dt switching level of 10-20 volts/microsecond. A transient anode voltage change at the rate of 10-20 volts/microsecond will cause the device to turn-on if reverse bias is not connected from gate to cathode. On the other hand, the GCS or GATT device will exhibit a dv/dt capability in excess of 400 volts/microsecond with bias applied. The ultimate level of sensitivity with bias is uncertain, since above 400 volts/microsecond the dv/dt generator source impedance is so low that turn-on by dv/dt is destructive. No devices have survived a test when turned-on by dv/dt with bias. Without a bias, dv/dt sensitivity is so low that the device is useless.

4.2.4 **Forward Conducting Voltage** - This parameter is measured in the standard fashion with an applied forward current pulse of 50 amperes which remains constant for several hundred microseconds. The GATT assumes a stabilized forward conducting voltage drop within several microseconds after turn-on. By contrast, a thyristor turns-on with a characteristic fall of anode voltage followed by a long spreading time. The lack of spreading effect in the forward voltage drop characteristic gives the GATT a transistor-like character.

The range of forward conducting drop for the GATT varies from 1.5 to 2.5 volts at the 50 ampere conducting level. These values are within the target range for the 50 ampere device.

4.2.5 **Latching Current** - Latching current is that value of anode current which must be assumed by a four layer device before continuation of the on state will remain after turn-on drive is removed. The latching currents for the GATT's ranged from 0.5 ampere to 35 amperes.

The devices with highest latch current were susceptable to failure if gate drive was not excessive. For this reason, measurements of minimum gate voltage-and-current-to-trigger were discontinued. Before latching, GATT device behavior resembles a transistor. Anode voltage will fall with gate current, and some indication of lack of latch may be determined from the tendency of the gate current to control conducting drop. For the smallest forward conducting drop before latching, gate current should be one-quarter of the anode current value. At high anode currents before latch, any transit from blocking state to conducting state will result in failure if gate drive is inadequate. For the present GATT design, a latching current of 10% of turn-off current capability is quite adequate.

4.2.6 Holding Current - Measured holding current values ranged from 0.5 milliamperes to 0.5 ampere.

4.3 Dynamic Measurements

4.3.1 Turn-On Time Measurements - The original assumptions regarding GATT turn-on were that the GATT would not possess a turn-on speed problem since the gate region surrounds the cathode islands. By analogy with thyristor turn-on characteristics, it was assumed that a GATT will turn-on at many points, resulting in a large turn-on area and high di/dt switching ability. A thyristor normally turns on at one spot since the gate layer of a thyristor is accessible only at one point, this point being the center of the structure for Westinghouse thyristors. By contrast, the GATT gate area surrounds the mesa-like cathode fingers. Hence, many cathode points are near the gate from which much charge may be supplied to promote injection. The GATT has been tested to show adequate turn-on for current rate-of-rise of 40-50 amperes per microsecond. For this load current rise, the GATT will turn-on in 1.0 microseconds. For circuitry in which current rise time is greater than 50 amperes per microsecond, the GATT will respond slower than the circuit speed and impede the flow of current. Here device limiting will occur causing the actual circuit response to be determined by the GATT instead of the external circuit. Device limiting is highly dissipative and is to be avoided, especially for high frequency switching duty. Figure 18

shows turn-on speed for a sample GATT for various levels of gate drive. For the largest gate drive of 16-18 amperes, turn-on occurs in 1.0 microseconds, but for lower drives turn-on is slower, so much that the current waveform is altered.

The turn-on illustrated by Figure 18 is not unusually swift; some units have recorded performance in the 0.5 microsecond area. The variation of turn-on speed with gate drive is typical and the characteristic as such presents a hazard area for high frequency duty. The most important point of turn-on characterization is the specification of current rate-of-rise with turn-on time.

4.3.2 Turn-Off Time Measurements - Circuit One - Original testing of turn-off time began with a simulation circuit with unique properties, see Figure 19. In this system, recovery of forward blocking ability occurs under the conditions of zero anode voltage and current. Although it was finally decided to concentrate test effort with a different circuit, the responses generated in the original simulation circuit of Figure 19 are of sufficient interest to be reported here.

In Figure 19, 50 amperes are diverted from the initially conducting loop (I_0) into the loop with the test device V(OUT). The current through the test device will remain at 50 amperes until the capacitor C_1 is charged to near the voltage V_1, at which time current will transfer back to the original conducting loop. During this transfer time the decay of current through the test device occurs at a rate of minus 10 A/μs. When the current through the test device reaches zero, a gate assist signal of -14 volts is applied by a transistor switch to the gate.

Figure 20 illustrates all the typical characteristics of the blocking junction recovery. Figure 20 is the behavior of the gate-cathode junction. At the instant of the application of gate assist voltage, a gate junction recovery current I_G flowing into the cathode can be observed. It quickly crests and the gate-cathode junction then recovers and starts to support reverse voltage. Considering the recovery of the blocking junction, it is obvious from Figure 20 that this junction does not recover as quickly as the gate-cathode diode, causing the anode

TURN-ON, DEVICE #6233

V_A - 200V/div

I_A - 20A/div

Hor. .5 μsec/div

I_g - 4A/div

Hor. .5 μsec/div
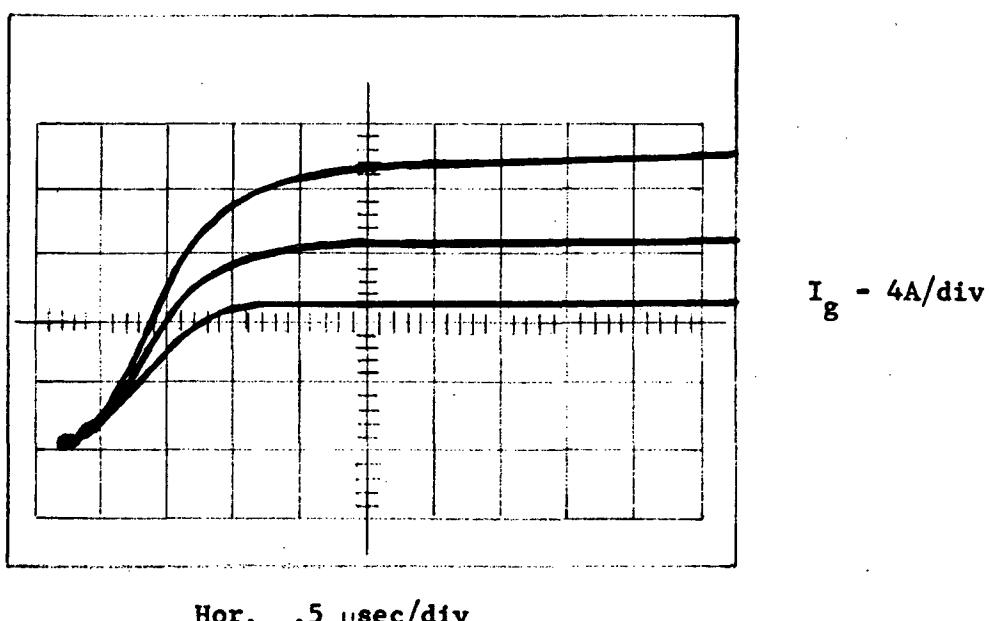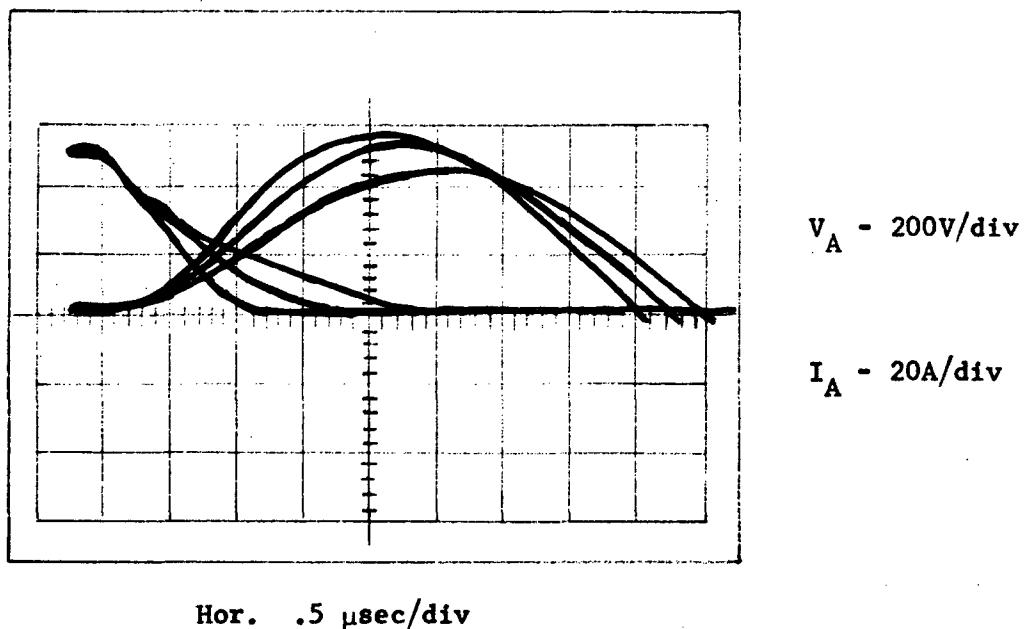
Fig. 18
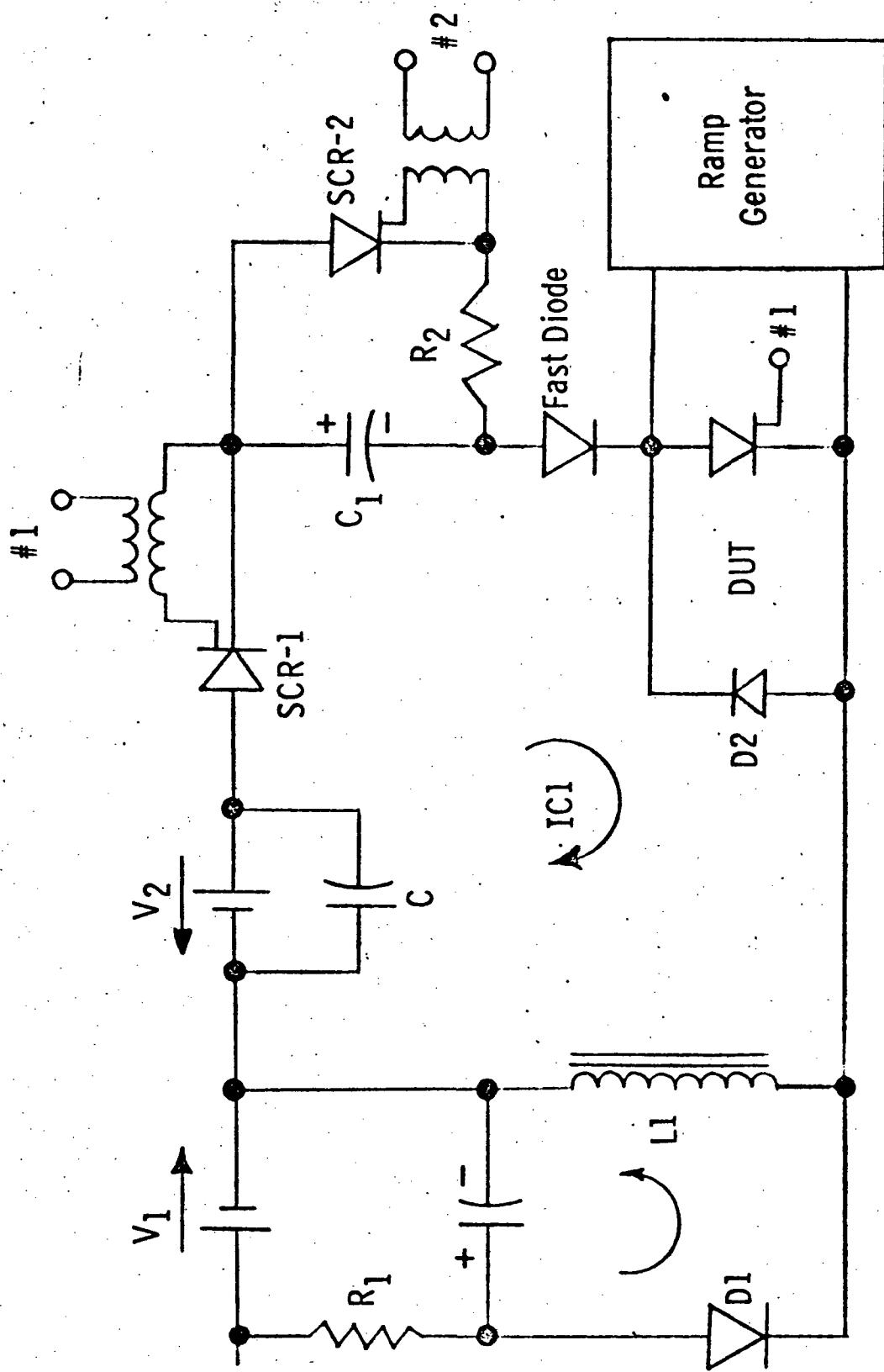
Electrical test circuit #1

Fig 19
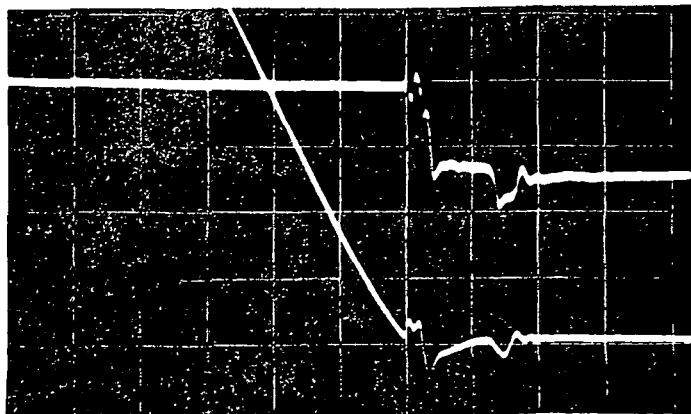
Fig. 20a

Top - Gate voltage 10V/div.

Bottom-Cathode current 5A/div.
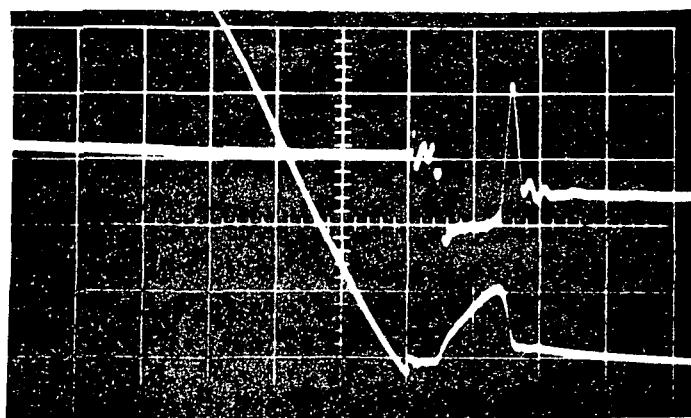
Fig. 20b

Top - Anode voltage 10V/div.

Bottom- Anode current 5A/div.
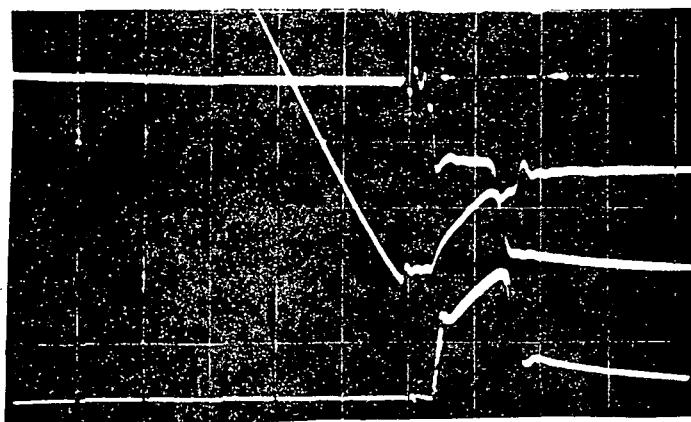
Fig. 20c

Top - Gate voltage 10V/div.

Mid - Anode current 5A/div.

Bottom - Gate current 4A/div.

Fig. 20. GATT Turnoff Waveforms
Sweep speed 1 μs/div.

to immediately drop to the gate potential of about -12 volts. With the anode 12 volts low, current begins to flow into the anode and out of the gate. It is assumed that the peak recovery current of the blocking junction observed in the anode lead is limited by external impedance of the anode circuit. When the anode current reaches this peak, normal blocking junction recovery occurs and a typical transient occurs at the anode at this point. After this recovery a small tail current still flows into the anode.

In Figure 20 the gate current, gate voltage and the anode current are shown simultaneously. The gate current pulse consists of a sharp leading edge due to rapid gate-cathode junction recovery and thereafter a slower rising front due to the higher circuit impedance in the diode circuit. The time from application of the gate assist signal to the instant of peak anode current is named t_{gr} and is considered to be the minimum obtainable blocking junction recovery time. Time t_{gr} is shown in Table 5 with peak anode current. It is clearly evident from these values that the blocking junction recovery time was reduced to less than 2 µs.

It was assumed that the peak recovery current in the anode was limited by the external circuit as in an ordinary diode circuit. Hence an additional diode D2 was added in the test circuit of Figure 19 to bypass any distributed inductance of the anode circuit. Figure 21a shows superimposed photos of the gate current pulse with and without bypass diode D2. Figure 21b gives the associated anode circuit and gate voltage waveshapes and Figure 21c shows clearly the effect of the inserted diode D2. With this diode, t_{gr} was decreased from 0.9 to 0.5 µs. The junction recovery time is then dependent on the device characteristics and on the gate assist voltage.

TABLE 5 GATT TURN-OFF TESTS

TURN-OFF TEST CIRCUIT NO. 1

$$T_c = 25°C$$

$V_g = -14V$ Applied at $I_a = 0$

| DEVICE	$T_{gr}/\mu s$	I_g Peak/Amps
56A3	1.0	8.0
56A7	.9	6.0
56F3	1.8	9.0
56F5	1.9	9.6
56F7	2.0	9.6
56D1	.8	6.0
51D12	1.3	7.2
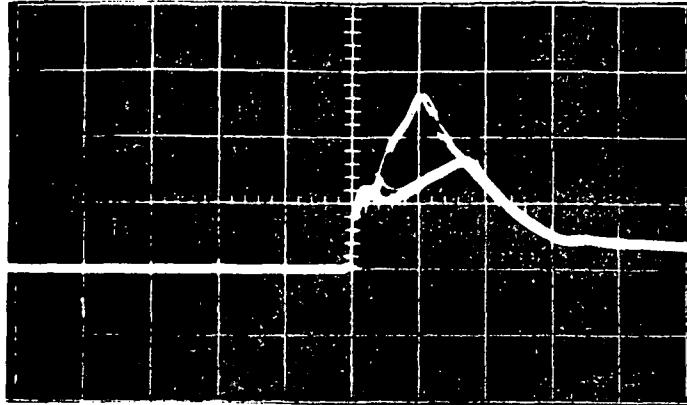
Fig. 21a

Top - I_G with diode D_2 4A/div.

Bottom - I_G without diode 4A/div.
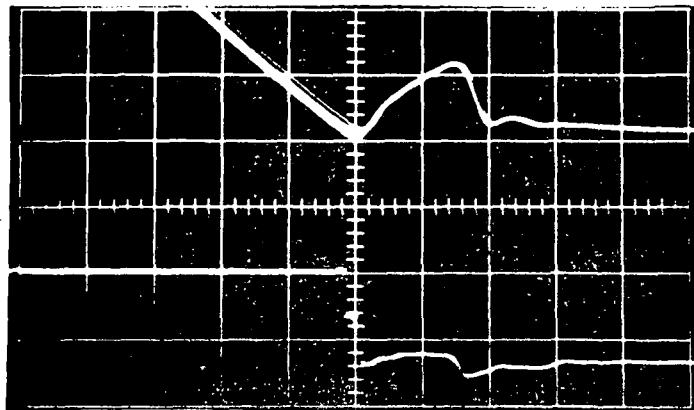

Fig. 21b

Top - Anode current without diode D_2
        5A/div.

Bottom - Gate voltage 10V/div.
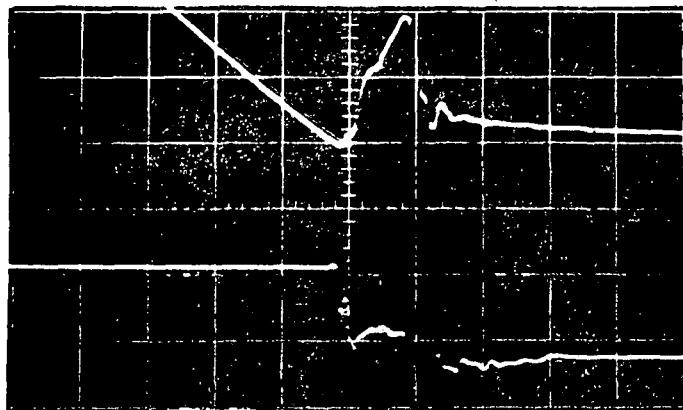
Fig. 21c

Top - Anode current with diode D_2
        5A-div.

Bottom - Gate voltage 10V/div.

Fig. 21. Effect of the bypass Diode D_2
on the GATT Turnoff Waveforms
Sweep speed 0.5μs/div.

4.3.3 <u>Turn-Off Time Measurements - Circuit Two</u> - Test circuit
2 is illustrated in Figure 22. An auxiliary thyristor T_1 charges the
capacitor C_1 to a preliminary voltage V_{CO}. After a delay to allow T_1 to
recover, the Device Under Test (DUT) is triggered, causing the discharge
of C_1 and the formation of a characteristic current pulse i_f. The circuit
Q is such that an induced voltage will appear across DUT, reversing its
polarity and turning it off. After another delay interval, T_1 is triggered
on and the cycle starts again. The circuit response values, V_{CO}, i_f peak,
the induced voltage V_R and the pulse length t_p are defined in Figure 22.

The performance of test circuit #2 is shown in Figure 23. The
major performance difference between the desired response and the one
observed is the magnitude of the induced voltage V_R. The specified value
was -50V whereas -160V was observed. This did not significantly alter
device performance.

The anode voltage and current responses are typical. Of
particular interest, especially for a device which is to operate under
high repetition rate conditions, is the magnitude of reverse recovery
current. From Figure 23, the duration of reverse recovery current is
several microseconds. The simultaneous occurrence of reverse recovery
current and reverse commutating voltage is dissipative and can add
significant device losses. It was observed that reverse anode recovery
current was dependent on the duration of forward gate drive pulse, see
Figure 24. These results show that recovery current will increase from
2.5 microseconds to 3.5 microseconds if a high amplitude gate drive is
maintained for the full conduction interval.

4.3.4 <u>Gate Assist Response</u> - For all operating conditions, a
bias voltage of -10 volts in series with 10 ohms was connected from gate
to cathode of the GATT device. The gate circuit response for this condition
is of importance immediately after the reduction of forward anode current.
It is also of interest to determine the gate circuit response when a low
impedance voltage source is switched to the gate at the instant forward
anode current reaches zero. These responses are illustrated in Figure 25,
the former labeled with subscript 1, and the latter with subscript 2.
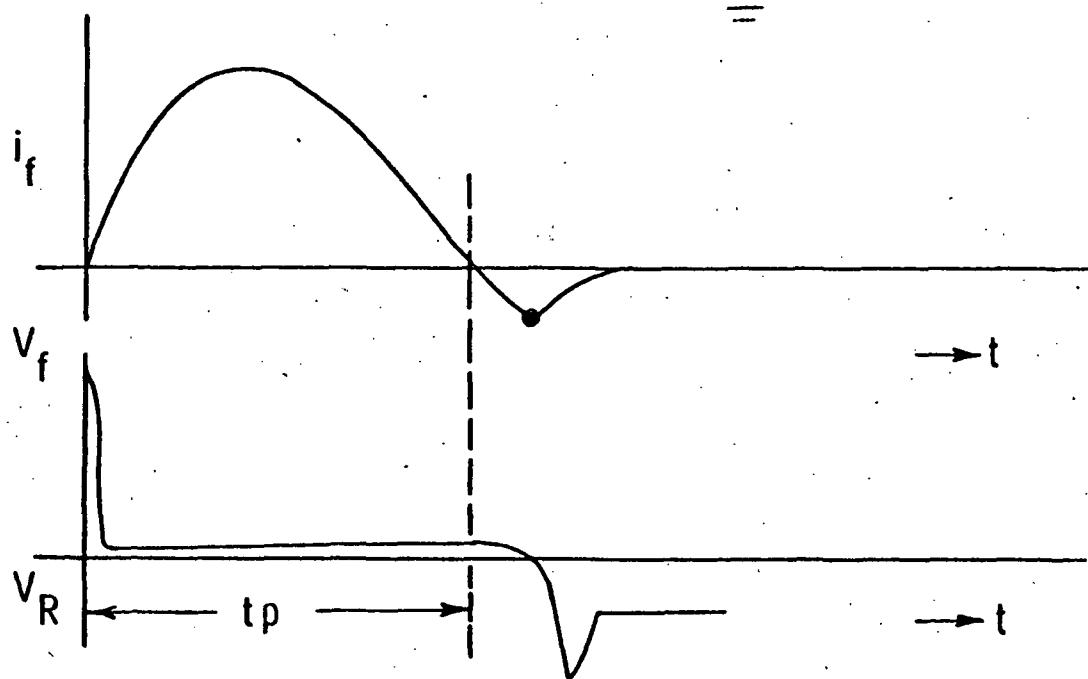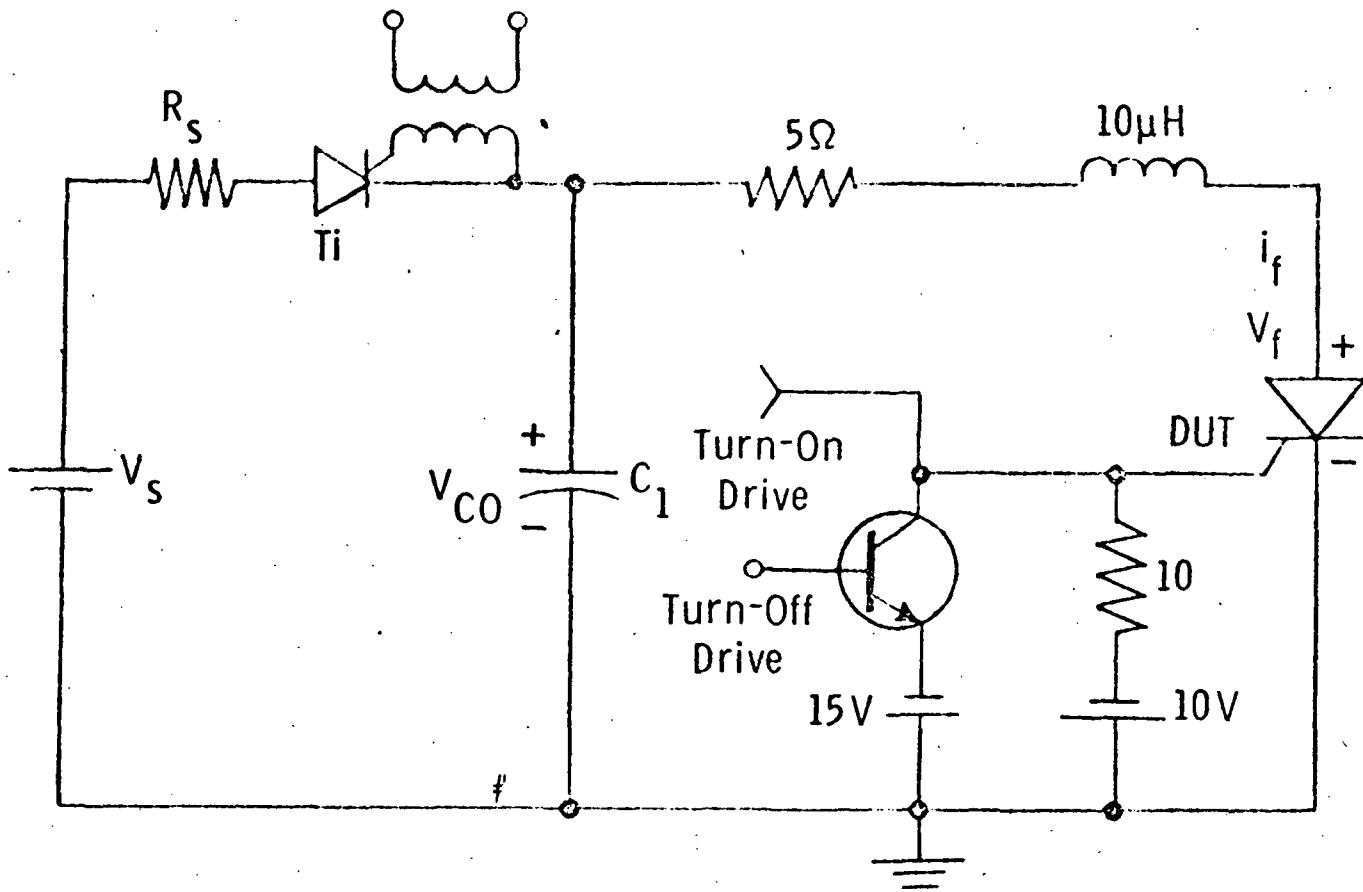
Gatts-Test circuit #2 with typical anode current and anode voltage V_F responses

Fig. 22

$$I_A = 20A/div.$$
$$V_A = 200V/div.$$

$$Speed = 5\mu s/div.$$
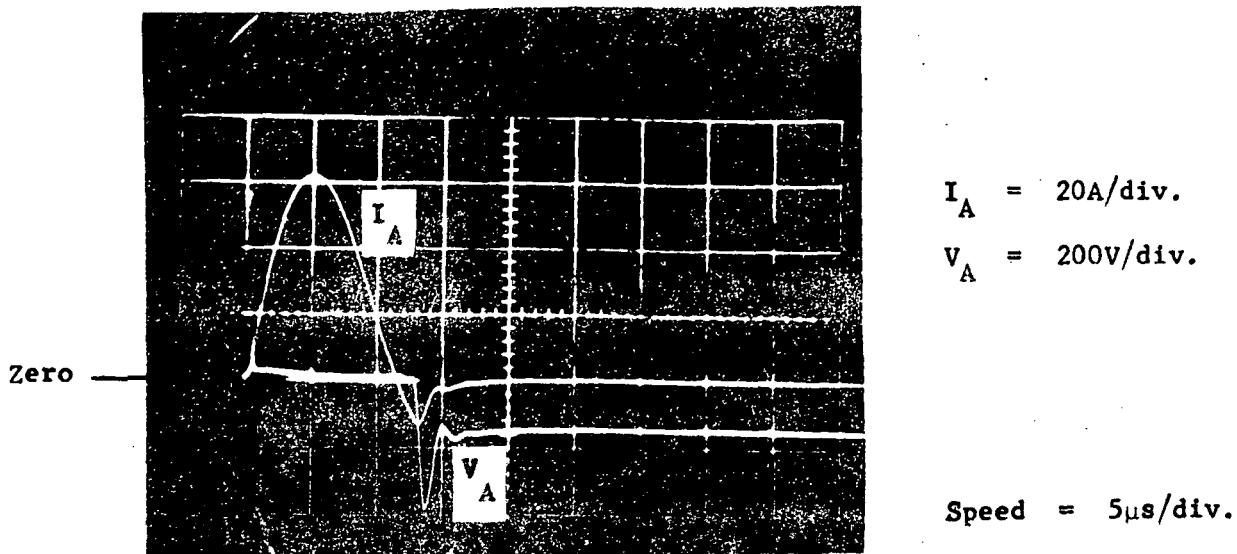
Fig. 23   Typical anode voltage and current of the
GATTS-unit when operated in test circuit #2

$$I_A = 20A/div.$$
$$I_g = 10A/div.$$
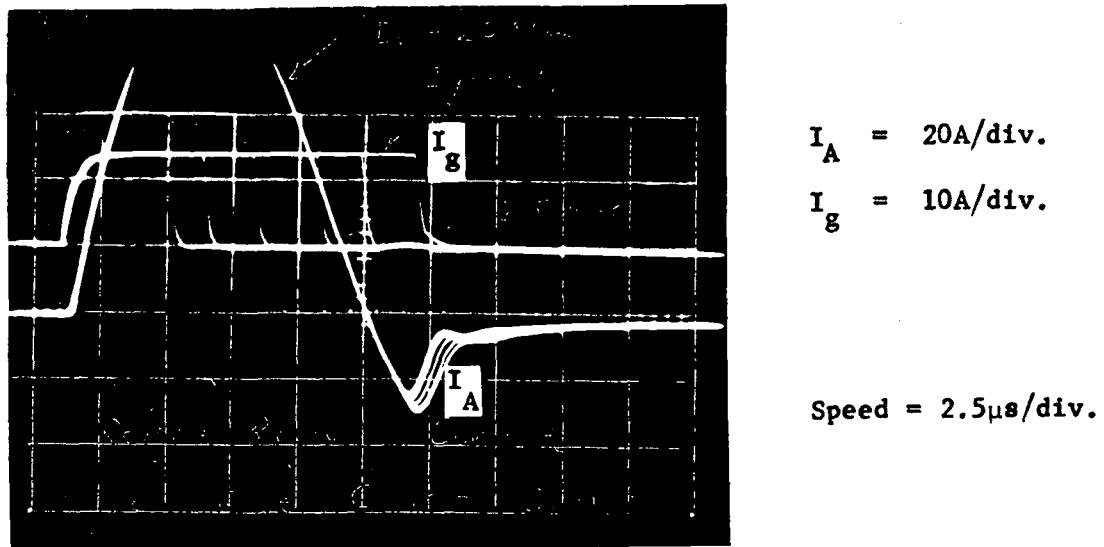
$$Speed = 2.5\mu s/div.$$

Fig. 24   Reverse anode recovery current as a function of
the length of the turn-on pulse

zero
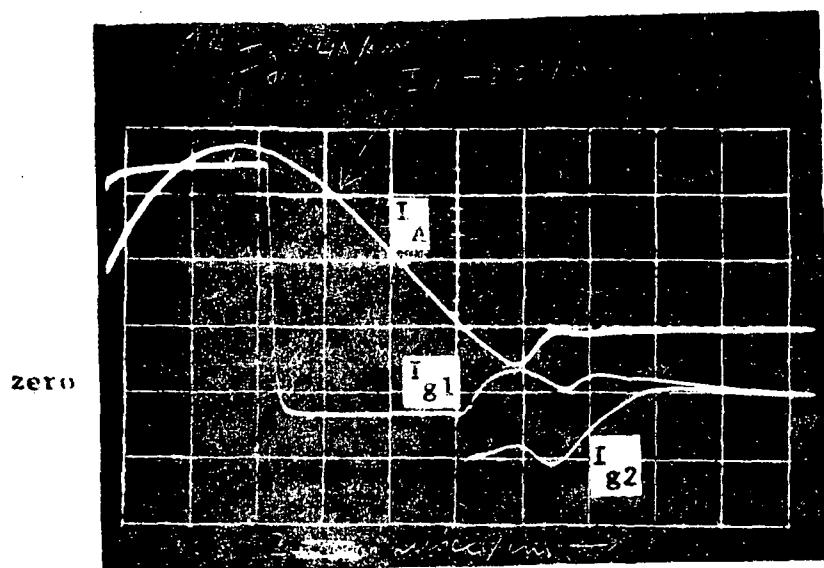
I_A = 20A/div.

I_{g1} = 4A/div.

I_{g2} = 4A/div.

Speed = 2µs/div.
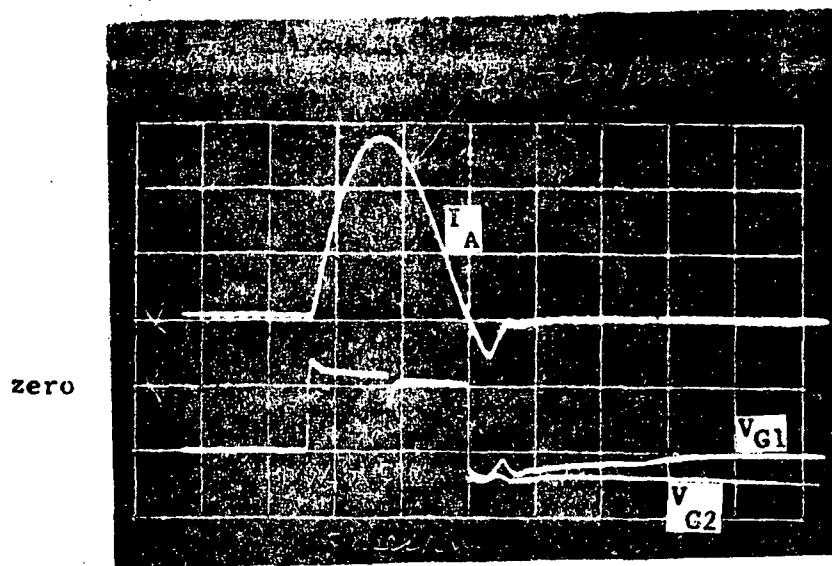
Fig. 25b

I_A = 20A/div.

V_{G1} = 10V/div.

V_{G2} = 10V/div

zero

Speed = 5µs/div.

Fig. 25. Gate current (a) and gate voltage (b) for a 10Ω/-10V and a -15V/pnp transistor gate drive circuit.

For I_{g1} the gate is continuously biased to -10V through a 10Ω resistor. Current I_{g2} arises from shorting the gate to a -15V source via an npn transistor when I_A reaches zero. It can be seen that the forward gate drive, which adds to the continuous bias, terminates slightly after I_A reached its peak. The gate voltage remain near zero while GATT is conducting positive anode current. During this interval a -1A gate current leaves the gate corresponding to the 10 volt drop across the 10Ω resistor. When I_A reaches zero, the gate starts to support voltage (Figure 25b) and positive I_{g1} flows. This is explained by the condition of the gate voltage when any level of reverse recovery current flows. Gate voltage V_{G1} is more negative than -10 volts. Hence for condition 1, a current will flow into the gate immediately after flow of forward current. This condition does not stimulate rapid blocking junction recovery.

When a low impedance voltage (V_{G2} -15 volts) is switched to the gate at forward current zero, some current may be extracted from the gate (I_{g2}). At this time, however, the extraction of current from the gate-base of the GATT is limited by the anode potential, which is negative (-160 volts), see Figure 23. It is concluded that the application of a gate assist potential at a time when the anode potential impedes the flow of forward junction recovery current is not an effective technique. Later testing will show that forward blocking recovery will be enchanced when a source of forward recovery current is available.

The application of a gate assist pulse to the gate of the device under test before anode current zero operates the GATT device in the gate control mode. By this technique the device will turn-off current. The anode voltage and current response for this condition is shown in Figure 26. The most serious effect is the rise of anode voltage when anode current is prematurely forced to zero. (Negative gate assist voltage is applied at the instant that anode voltage rises). The anode voltage rise results from current flowing in the resonant inductance of the anode current loop. Premature reduction of anode current by gate control results in release of $1/2$ LI_θ^2 energy which is dissipated in the device. The excess device dissipation is clearly not tolerable.

Device #56F7
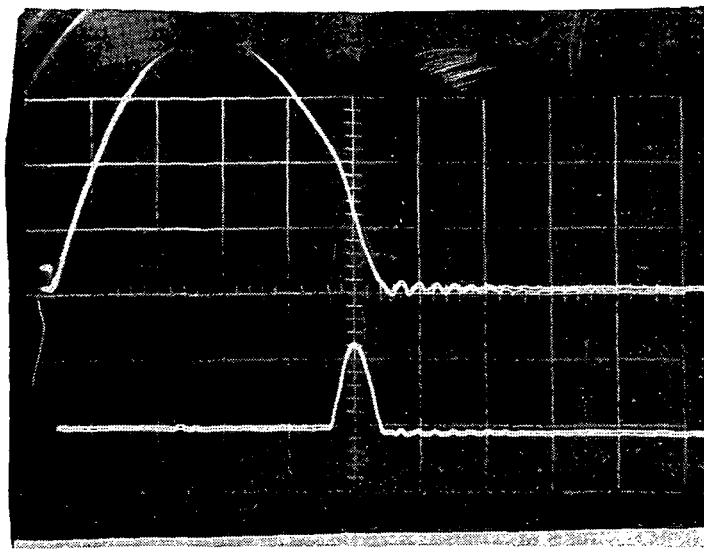
I_A - 10A/div.

V_A - 200V/div.

Figure 26. Gate-Assist Thyristor
Operating Turn-off Mode

4.3.5 <u>Turn-Off Time With Reverse Current</u> - For the turn-off test of the GATTS device the circuit of Figure 22 was modified such that a thyristor SCR1 was inserted in series with DUT, see Figure 27. The purpose of SCR1 is to isolate the forward current loop of Figure 22 from the reapplied voltage circuit. Thyristor SCR1 and DUT are triggered simultaneously. The isolation thyristor is selected to have a recovery time longer than that of the test GATT device (DUT). Therefore, DUT will develop and support all reverse voltage provided by capacitor C_1 of Figure 22. However, thyristor SCR1 must recover before DUT will support reapplied forward voltage, and in so doing draws some reverse recovery current. As a consequence, some distortion of the reapplied voltage occurs.

For testing purposes, it has been prudent to keep the impedance level of the reapplied voltage source as high as possible. I. turn-on occurs due to insufficient recovery time, a high impedance reapplied voltage source prevents destructive failure. As a second concern, high reapplied voltage rates require low driving point impedance because of line and device capacitances. Hence, the impedance of the reapplied generator is chosen as a compromise of these factors. The response of a GATT device to gate assist and reapplied voltage is shown in Figure 28. Anode current and voltage responses are shown in Figure 28a. The anode current waveform shown is the tail end of the forward anode current when anode current reaches zero, and thereafter. (A cross indicated current zero). The typical reverse current is shown after current zero, followed by a sequence of pulses of current which flows into the anode of the GATT device. These pulses are forward recovery current pulses caused by reapplied voltage pulses applied at the instants shown in the lower portion of Figure 28. The characteristics of forward recovery current are similar to those of reverse blocking junction recovery. At the instant reapplied voltage is applied to the anode of the test device, forward recovery current flows into the anode. The anode of the test device remains clamped to near zero volts until recovery of the forward blocking junction. At this
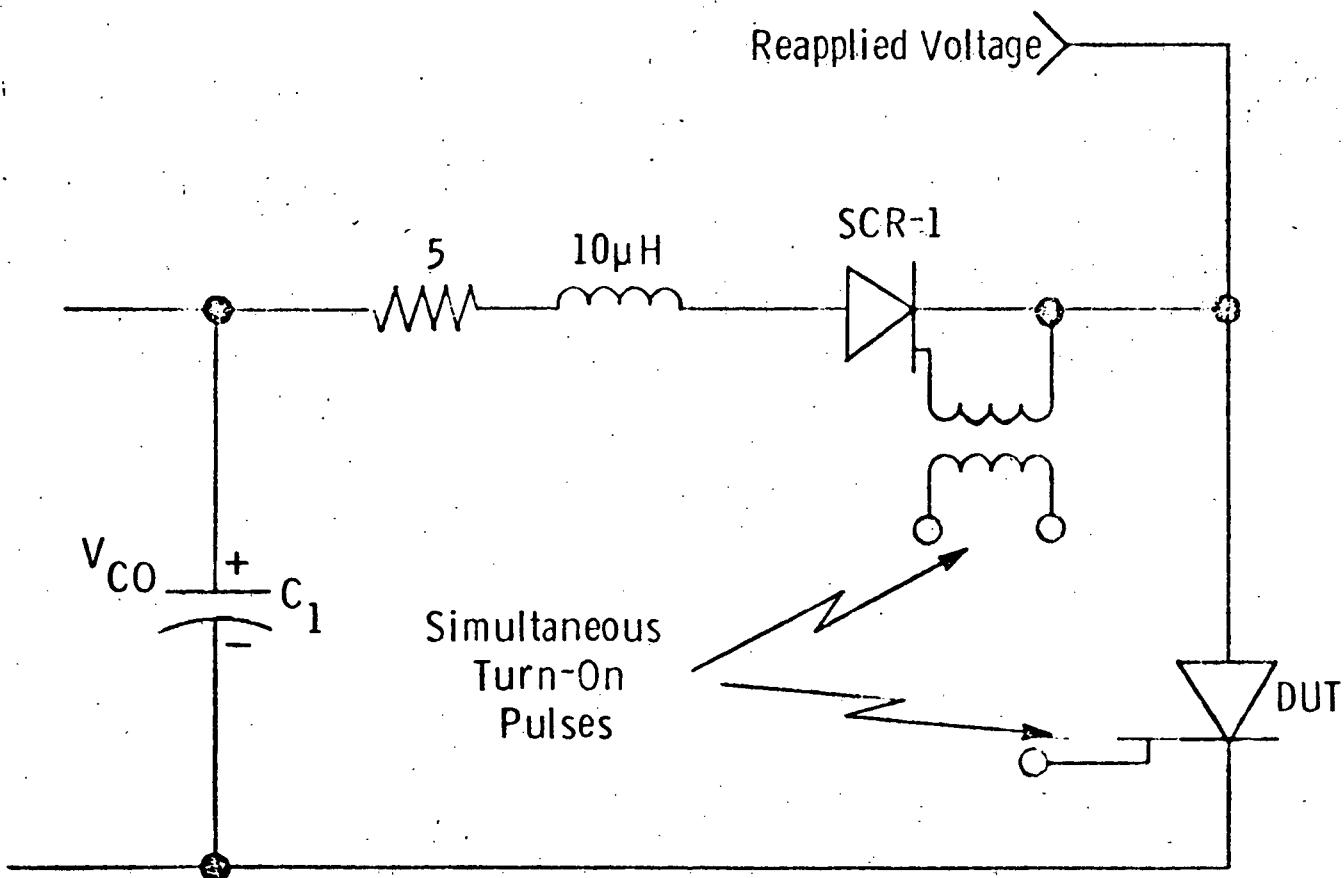
Test circuit # 2 modification with SCR-1 for isolation of reapplied voltage source

Fig. 27

I_A - 5A/div.

V_A - 200V/div.

Hor. - 2μs/div.

Figure 28a

I_g - 4A/div.

V_A - 200V/div.

Hor. - 2μs/div.
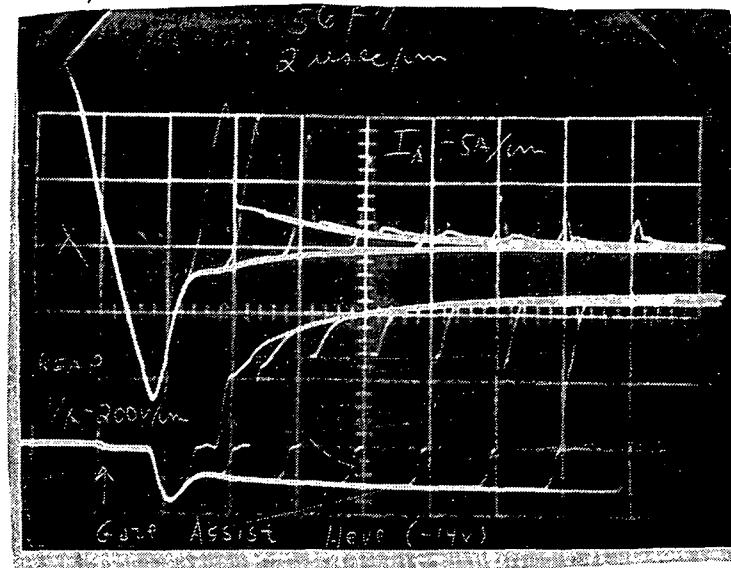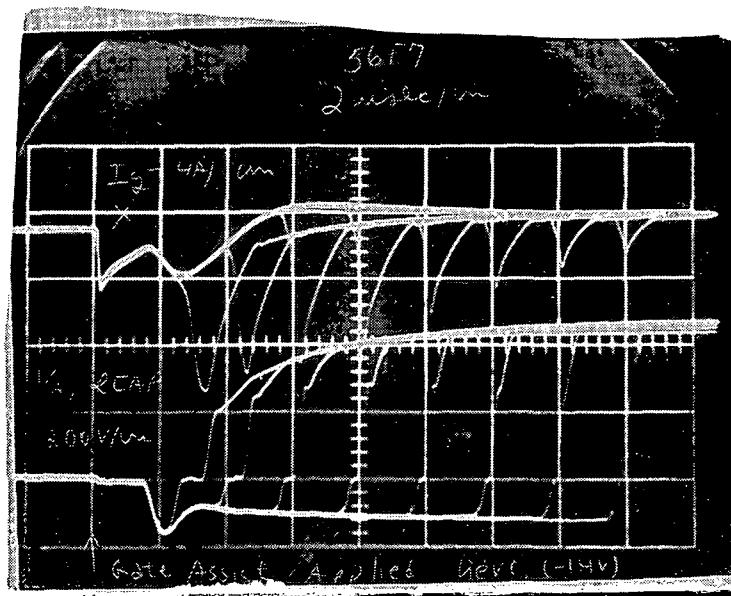
Figure 28b. Turn-off Time Response with Gate-Assist

point, anode current peaks, and forward anode voltage begins to rise. At a higher anode voltage level, the voltage across the isolating thyristor SCR1 changes from forward to reverse, causing a small distortion of the reapplied signal. The fastest recovery time shown in Figure 28 is 3.5 microseconds. A faster recovery time in this simulation would require application of forward reapplied voltage to the test device before reverse recovery of the isolation thyristor SCR1. To increase the anode voltage under these conditions would require rapid charge of discharge capacitor C1 from the high impedence reapplied voltage source. This was not possible and a second technique was used to determine minimum recovery time. It will be discussed at a later point in this report.

Figure 28 illustrates gate current response for reapplied voltage excitation. Clearly, forward anode recovery current is extracted by the gate. Note that the gate current of Figure 28 is the same as I_{g2} of Figure 15, with the addition of extracted gate current. Also the reapplied voltage pulse is in excess of 400 volts per microsecond.

4.3.6 Turn-Off Time With Small Reverse Current - As a final measure of GATT device capability, a test was devised for which minimum recovery time could be measured. In the simulation circuit, minimum recovery time is determined by the recovery time of the forward current isolation device. For the response of Figure 28, the isolation device was SCR1 of Figure 27. For the final test, SCR1 is replaced with a fast recovery diode such that most recovery current is nearly eliminated, as well as the reverse voltage developed across the test device. Since the speed of the isolation diode is much faster than the test device, all reverse voltage will be supported by the isolation diode, and none by the test device. It is generally assumed that reverse current will hasten blocking recovery. The elimination of reverse current is then more severe than a recovery test with reverse current available. The test responses are shown in Figure 29.

I_A - 5A/div.

V_A - 200V/div.

Hor. - 2μs/div.

Figure 29a

I_g - 4A/div.

V_A - 200V/div.

Hor. - 2μs/div.
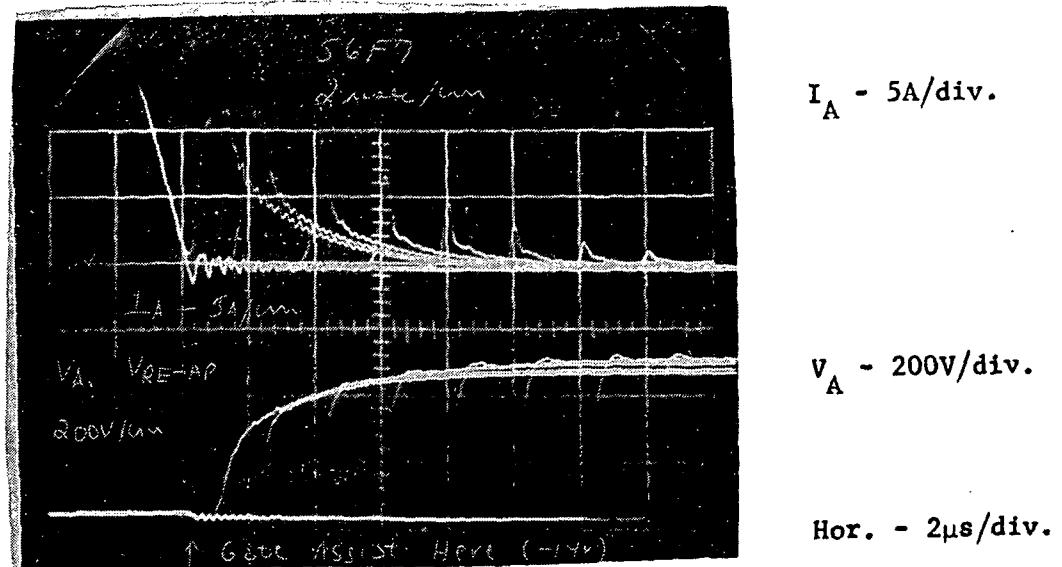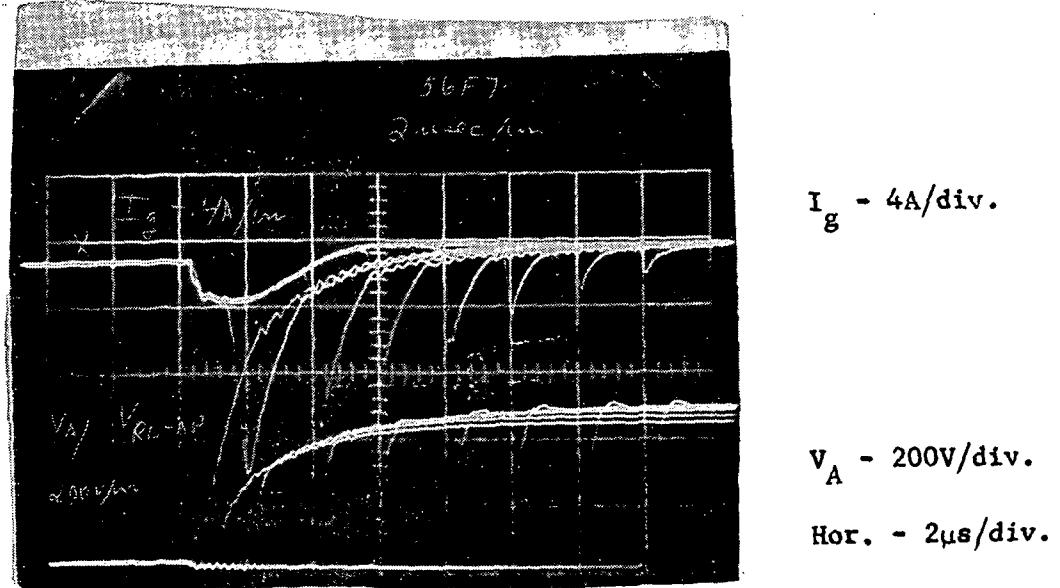
Figure 29b. Turn-off Time Response with Gate Assist -
No Reverse Current.

- 75 -

Minimum recovery time is one microsecond. This is clearly related to the rise time of the minimum recovery current which reaches a 14 ampere peak and begins to flow at the instant forward current reaches zero. The data of Figure 28 is typical performance at 100°C case temperature.

The sequential photographs of reapplied voltage at various instants illustrate the decaying character of forward recovery current. As time progresses after forward current zero, carriers trapped within the device junctions decay by recombination, causing the observed reduction of recovery current. The large recovery current pulse at minimum recovery, in coincidence with reapplied voltage is dissipative and will have some influence upon the frequency rating of the GATT device.

4.4 Conclusions

Performance tests conducted at the Westinghouse R&D Center indicate that thyristor-like devices may be fabricated with measurable recovery times of less than two microseconds. Although not measured by the exact and conventional test system, a test technique was devised with test conditions considered more severe than normal. The results of these tests were excellent.

Other test results of the gate assisted turn-off thyristor are good. Some compromise of turn-on characteristics was evident, requiring higher drives than normal to achieve reasonable turn-on. The resultant turn-on is considered less dissipative than that of a simple thyristor in that the spreading effects normally associated with single point thyristor turn-on are absent. Hence, although the GATT turns on slower than a thyristor, complete turn-on is achieved faster.

Most characteristics of the GATT device are comparable to those of an ordinary thyristor. The devices perform the gate assisted turn-off function very well indeed. The dv/dt capability is in excess of 400V/μs and the minimum recovery time is less than 1 μs.

5. DEVICE DATA

In this section we present three major sets of data. The first are the specifications on four devices shipped to NASA(ERC) some four months after the commencement of the contract. These devices did not meet all of the specs, specifically missing the blocking voltages, but they are nevertheless indicative of the quality of some of the first units produced. The second data are on the nine devices that were rather fully characterized part way through the contract. Some of these devices were used as the device under test in Section 4. The third data are the devices delivered to NASA Lewis. These data are tabulated in Tables 6, 7&8, and 9 respectively.

Table 6--Characteristics of First Four GATT Devices
(These devices are typical of early 50A units.
They were delivered about 4 months after the
start of the contract.)

No.	V_{FB}/V	@ mA	V_{RB}/V	@ mA	V_{GRB}/V	@ mA	V_F/V 50A	I_{GTO}/A	$t_{off}/\mu s$	$t_{on}/\mu s$
1	600	15	500	10	16	0.5	2.3	18	2	4
2	800	< 10	650	< 10	16	0.1	2.2	18	2	3.5
3	600	10	250	< 10	16	< 0.2	2.2	20	2	3
4	810	10	350	< 10	16	2.0	4.4	18	2	3

Table 7--GATT Static Voltage Tests for Nine Devices

Device		V_{FB} @ 25°C		V_{FB} @ 100°C		V_{RB} @ 25°C		V_{RB} @ 100°C		V_{GR} @ 25°C		V_{GR} @ 100°C		Comments
		Volts	mA	Volts	mA	Volts	mA	Volts	mA	Volts	mA	Volts	mA	
51E11	OG	490		200		550		300	2	16	.05	17.2	.5	Failed
	10ΩG/C	485		200										
56A3	OG	780		500		210		100		14.8	.5	15.2	.4	
	10ΩG/C	830		730										
56A7	OG	400	2	300		150		100		15	200	15.8	200	
	10ΩG/C	420	2	300										
56F2	OG	680	2	630	7	480		475		14	.2	14.8	.5	Failed
	10ΩG/C	680	2	775										
56F3	OG	500	4	400		400		340		14	20	15	20	
	10ΩG/C	500	3	600										
56F5	OG	970		790	4	470		510		14	.2	15	1	
	10ΩG/C	1000		1000										
56F7	OG	850	2	700	6	520		430		14	1	14.6	2	
	10ΩG/C	970	1	900	8									
56D1	OG	780	2	720	5	380		480		14	160	15	150	
	10ΩG/C	800	2	850										
51D12	OG	750		570	3	260		150	3	16	.2	18	300	Failed
	10ΩG/C	770		560										

NOTE: OG - Open Gate
10ΩG/C - 10Ω Gate/Cathode

Table 8--GATT Dynamic Evaluation

Device	I_{HO}/mA V_a = 6V dc T_c = 25°C	I_{LX}/A V_a = 6V dc T_c = 25°C	V_F/V @ I_A = 50A T_c = 25°C	dv/dt V/μs @ T_c = 100°C Gate 10Ω/-10V	Gate Open
51E11	175	3.7	1.9	Failed	40
56A3	60	0.96	1.2	> 300	15
56A7	50	1.25	1.4		15
56F2	40	0.55	1.15	> 300	
56F3	50	0.60	1.2	> 300	
56F5	45	0.66	1.4	> 300	18
56F7	70	0.86	1.6	> 300	20
56D1	110	1.9	1.8	> 300	40
51D12	110	1.5	1.5	> 300	30

Table 9. Electrical Characteristics of Devices Delivered to NASA Lewis

Unit No.	BLOCKING STATE 25°C Data V_{FB} Volts	I_{FB} mA	V_{RB} Volts	I_{RB} mA	100°C Data V_{FB} Volts	I_{FB} mA	V_{RB} Volts	I_{RB} mA	CONDUCTING STATE Forward Voltage @ 25°C Volts	REVERSE GATE CHARACTERISTICS V_{GR} @ 25°C Volts	I_{GR} @ 25°C mA	Maximum GATT Turn Off @ 100°C μsec.
52A7	600	0.05	600	0.05	600	5.0	600	5.0	2.3	--	---	2.0
52B14	600	0.05	470	0.05	600	5.0	600	5.0	1.8	--	---	2.0
52D4	600	0.05	600	0.05	600	5.0	600	5.0	1.7	--	---	2.0
71-7	600	0.05	600	0.10	600	2.0	600	3.0	2.0	11	250	2.0
77-2	600	0.40	600	0.05	600	1.0	600	2.0	1.4	14	70	2.0
77-3	600	0.05	600	0.05	600	5.0	600	5.0	2.0	13	150	2.0
77-7	600	0.05	600	0.05	600	5.0	600	5.0	2.0	14	60	2.0
77-8	600	0.05	600	0.05	600	1.0	600	3.0	1.4	14	70	2.0
77-13	600	0.05	600	0.05	600	1.0	600	3.0	1.4	12	75	2.0
77-14	600	0.05	570	0.05	600	2.0	200	3.0	1.8	12	50	2.0
78-1	600	0.05	600	0.05	600	2.0	600	10.0	1.8	14	40	2.0
79-4	600	0.05	600	0.05	600	5.0	600	5.0	2.0	15	75	2.0
79-5	600	0.05	600	0.05	600	5.0	600	5.0	2.0	15	125	2.0
79-10	600	0.05	600	0.05	600	5.0	600	5.0	2.0	16	4	2.0
79-12	600	0.05	600	0.05	600	5.0	600	5.0	2.0	16	60	2.0
80-21	600	0.05	600	0.05	600	2.0	600	2.0	1.8	16	>1000	2.0
80-27	600	0.05	600	0.05	600	2.0	600	4.0	1.8	12	600	2.0
80-29	600	0.05	600	0.05	600	2.0	600	3.0	1.8	16	>1000	2.0
80-42	600	0.05	600	0.05	600	5.0	600	5.0	2.0	16	>1000	2.0
80-49	600	0.05	270	2.00	600	1.5	260	5.0	1.8	12	150	2.0
80-61	600	0.05	600	0.05	600	5.0	600	5.0	2.0	12	500	2.0
80-131	600	0.05	600	0.05	600	1.0	600	3.0	1.8	12	10	2.0

6. CONCLUSIONS AND RECOMMENDATIONS

Exceedingly fast, gate-assisted thyristors can indeed be made. The proper philosophy, design and development can lead to devices which recover within 2 µs after the natural commutation of anode current and in face of a reapplied voltage of 400 V/µs. The average forward drops are about 2 V at 50A forward current, again within the requirements of the proposal. Also, we now have a very good understanding of the problem areas in these devices. The opportunities lie clearly in the direction of more uniform processing, for with more uniform processing the sweep-out capabilities of the multiple gates will be more readily utilized and the performance of the whole device will more closely approximate the sum of its parts. There is every indication that 2 µs GATT units should be able to recover from peak currents in excess of 100A at these blocking voltages, forward drops and temperatures. It is our recommendation that the next step be towards higher current devices and towards a better package for these units. Airborne or space applications are better served by a Pow-R-Disc than a stud-mount device and there is every reason to believe that a GATT device should function better in such a low inductance pack. The goal of a lightweight, high efficiency series inverter with three times or four the present capability is attractive indeed.

7. NEW TECHNOLOGY

The principal item of New Technology resulting from this work was the demonstration that the contract objectives were feasible. Devices meeting the specification were produced.

Maximum Forward Blocking Voltage	Volts	V_{FB}	600
Maximum Reverse Blocking Voltage	Volts	V_{RB}	600
Maximum Forward Drop at $I_A = 50A$	Volts	V_F	2.0
Maximum Junction Temperature	$^{\circ}C$	T_j	125°
Maximum Crest Anode Current	A	I_A	50
Recovery Time (See Fig. 4) after $I_A = 50A$ is circuit commutated off	μs	t_r	2
Maximum Initial Rate of Reapplied Voltage Use Exponential to V_{FB} Maximum at $T_j = 100^{\circ}C$	V/μs	dV_{RM}/dt	400
Maximum Rate of Current Removal	A/μs	di/dt	10

A significant New Technology was also demonstrated in the use of bonded wires parallel to the silicon surface for selective contact of power device elements in a compression-bonded (CBE) package. While probably not economically feasible in high volume manufacturing, the technique is of significant value in power device engineering, since power devices typically cannot be tested in full or in part until they have been provided with proper thermal contacts. The selective bonding - CBE approach greatly simplifies the measurement of developmental units.

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